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(57) Abstract :

Abstract: The invention discloses architecture of reversible logic ALU with parity preservation, which will be a better alternative technology to overcome .the drawbacks current CMOS technology in digital logic circuits. The architecture comprises of parity preserving ALU in reversible logic, by incorporating ALU with complex arithmetic and logical functions. The logic gates in the ALU are designed using the KMD Gate that encompasses the reversible logic functions for those gates. The architecture consists of an input module that passes the control signals and data to the data processing module. Complete reversible logic functionalities for arithmetic and logical operations are implemented in the data processing unit. The functional modules in the data processing unit forward the computed results to the output module, with the support of the select lines. The evaluated performance of the ALU is quantum cost 293, constant input 41, garbage output 77 and total cost 411. The invention offered here is a supplementary feature for modern digital integrated circuits, to enable high speed operations using the invented reversible logic gates. This architecture would certainly be helpful in achieving an active step towards the implementation of an add-on feature towards modern day digital logic circuits.

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