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# Symmetric and Asymmetric Multilevel Inverter Topologies with Device Count: A Review

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**Abstract**

Multilevel Inverters, due to its high power and high voltage delivering capability have created a vast area of research in power electronics. The reduction in device count in these inverters has increased its efficiency to a much higher level. This has increased the interest in deriving new multilevel inverters with optimum device count. In this paper some of the recently proposed multilevel topologies with reduced device count for symmetric and asymmetric topologies are compared for their compatibility and advantages. The comparison will help in the choice of new topologies for different applications with better performances. The comparison is done for 31 level multilevel inverters which can be supplied from renewable energy resources, fuel cells etc.

***Keywords:***Multilevel Inverter, H-bridge, symmetric topology, asymmetric topology, output voltage.

# 1 Introduction

Inverters are devices that convert DC power into AC power from the available source. Multilevel inverters are devices that are used for high power conversion from the available DC source. These inverters produce stepped output voltage from the input DC sources. The quality of this output voltage increases with the increase in the number of steps or levels. Usually the level of a multilevel inverter is accounted as the total number of steps in the output voltage in one full cycle along with the zero level. There are mainly three basic structures presented for multilevel inverter topology: Diode clamped multilevel inverter, Flying capacitor multilevel inverter and cascaded multilevel inverter. Cascaded multilevel inverter has received more attention when compared to other two topologies. Because it has simple structure, modular design and easy to expand the level of output voltage [1] - [3]. In basic cascaded multilevel inverter[4],each H-bridge consists of four switches and produce three level of output voltage such as +Vdc, 0 and -Vdc. By adding additional H-bridge the output increases to next level. But when number of level increases the complexity of the system also increases. The application of cascaded multilevel inverter is limited due to the requirement of separate DC sources (SDCS) and number of semiconductor devices[4]. To overcome such limitations, many topologies have been proposed nowadays based on basic cascaded multilevel inverter [5]-[31]. Multilevel inverters are classified into symmetric and asymmetric topologies depending on the magnitude of the DC voltage sources. The efficiency of these inverters depend highly on the number of devices used in its structure. Hence there is greater interest in deriving new topologies from the basic structures with reduced device count. This in turn reduces the switching losses and eliminates the lower order harmonics. The decrease in number of insulated gate bipolar transistors (IGBTs) further reduces the cost of the inverter. These power switches are controlled so as to aggregate these multiple input DC levels to obtain high voltage at the output.

# 2 SYMMETRIC TOPOLOGIES

In Symmetric multilevel inverter topology, the magnitude of all dc voltage sources are equal. Three topologies are discussed in the following section which are capable of working only in symmetrical topology.

A. Symmetric MLI by Choi and Kang in 2009

The topology proposed in [5, 6] describes about a series connected switched sources based MLI. In this topology sources connected in series through power switches. The topology comprises of an H-bridge to impart positive and negative polarities. This H-bridge based MLI for Nlevel is shown in Fig. 1. The number of DC voltage sources and switches used in this topology increases accordingly with levels.

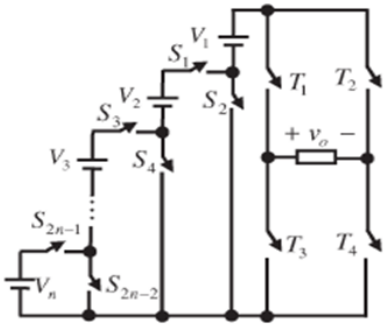


Fig. 1. Symmetric MLI by Choi and Kang in 2009

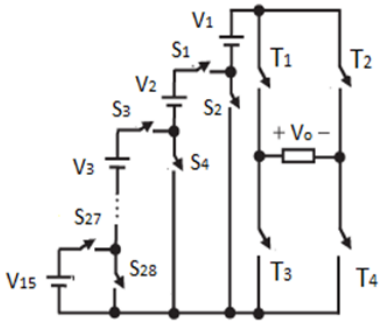


Fig. 2. Symmetric MLI by Choi and Kang in 2009 for 31 level

The effective number of output phase voltage levels (Nlevel) in this topology may be related to the number of separate dc sources (N) by Nlevel = 2N+1 and the number of switching devices is given

by Nswitch = 2N+2. The maximum output voltage (Vo.max) of this proposed symmetric multilevel inverter is NVdc. Fig. 2 shows the topology for 31 level. The possibilities of synthesizing various combinations of input DC levels for 31 level output are summarized in Table 1.

Table 1: Switching States of the Symmetric MLI proposed by Choi and Hang for 31 Level

| State | Output voltage | Switches in ON State |
|---|---|---|
| 1 | $V_{dc}$ | S2 |
| 2 | $2V_{dc}$ | S4,S1 |
| 3 | $3V_{dc}$ | S6,S3,S1 |
| 4 | $4V_{dc}$ | S8,S5,S3,S1 |
| 5 | $5V_{dc}$ | S10,S7,S5,S3,S1 |
| 6 | $6V_{dc}$ | S12,S9,S7,S5,S3,S1 |
| 7 | $7V_{dc}$ | S14,S11,S9,S7,S5,S3,S1 |
| 8 | $8V_{dc}$ | S16,S13,S11,S9,S7,S5,S3,S1 |
| 9 | $9V_{dc}$ | S18,S15,S13,S11,S9,S7,S5,S3,S1 |
| 10 | $10V_{dc}$ | S20,S17,S15,S13,S11,S9,S7,S5,S3,S1 |
| 11 | $11V_{dc}$ | S22,S19,S17,S15,S13,S11,S9,S7,S5, S3,S1 |
| 12 | $12V_{dc}$ | S24,S21,S19,S17,S15,S13,S11,S9,S7,S5, S3,S1 |
| 13 | $13V_{dc}$ | S26,S23,S21,S19,S17,S15,S13,S11,S9, S7,S5,S3,S1 |
| 14 | $14V_{dc}$ | S28,S25,S23,S21,S19,S17,S15,S13,S11, S9,S7,S5,S3,S1 |
| 15 | $15V_{dc}$ | S27,S25,S23,S21,S19,S17,S15,S13,S11, S9,S7,S5,S3,S1 |
| 16 | 0 | T1T3(or) T2T4 |

This symmetric topology needs twenty eight switches along with the four H-bridge switches to create 31 level output waveform. The main disadvantage of this symmetric system is that, as the level increases, the size of the inverter also increases linearly. This in turn increases the conduction losses and also the switches conducting for the lower levels have to conduct for all the levels. Thus stresses on these switches are high. This topology does not offer any possibility of employing asymmetric source configurations for further reducing the switch count.

Note: For symmetric topology,

V1=V2=..=V15=Vdc

T1 and T4 is switched on for positive half cycle and T2 and T3 is switched on for negative half cycle.

B. Symmetric MLI by Babaei et.al in 2012

This symmetric topology proposed in [9-11] consist of two parts. One part is the level creator part that generates the voltage level. The dc sources are separated from each other by a power switch so that it can be conducted or bypassed for producing the required output voltage level. The output voltage of the level creator part is always positive. The other part is the H-bridge which is required to create zero and negative output levels. The Fig. 3 shows the symmetric topology proposed by Babaei et.al for Nlevel. The switches used in this symmetric topology are bidirectional. According to the authors, this topology can only improve the performance of the inverter rather than reduction in the number of devices. The effective number of output phase voltage levels (Nlevel) in this topology may be related to the number of separate dc sources (N) by Nlevel = 2N+1 and the number of switching devices is given by Nswitch = 2N+2. The maximum output voltage (Vo.max) of this proposed symmetric multilevel inverter is NVdc

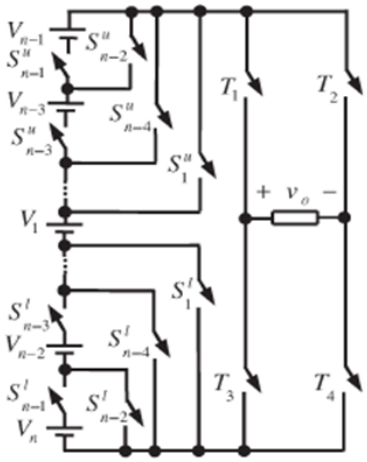


Fig. 3. Symmetric MLI by Babaei et.al in 2012

Fig. 4 shows the proposed topology for 31 level. The number of switches required for 31 Level MLI is thirty two. The switches in the upper half are subscripted as U and the switches in the lower half are subscripted as L for simplicity. Also there are many possible ways to generate different levels with different switches. The switching states of the topology for 31 level is shown in the Table 2.

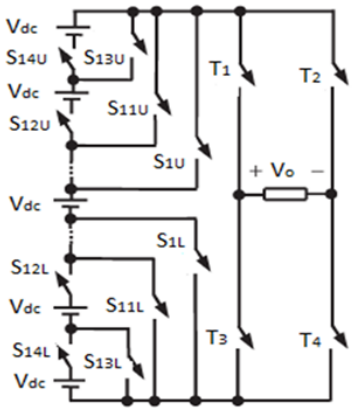


Fig. 4. Symmetric MLI by Babaei et.al in 2012 for 31 level

Table 2: Switching States of the Symmetric MLI proposed by Babaei et.al for 31 Level

| State | Output voltage | Switches in ON State |
|---|---|---|
| 1 | Vdc | S1L,S1U |
| 2 | 2Vdc | S3U,S2U,S1L |
| 3 | 3Vdc | S3U,S2U,S2L,S3L |
| 4 | 4Vdc | S5U,S4U,S2U,S2L,S3L |
| 5 | 5Vdc | S5U,S4U,S2U,S2L,S4L,S5L |
| 6 | 6Vdc | S7U,S6U,S4U,S2U,S2L,S4L,S5L |
| 7 | 7Vdc | S7U,S6U,S4U,S2U,S2L,S4L,S5L, S7L |
| 8 | 8Vdc | S9U,S8U,S6U,S4U,S2U,S2L,S4L, S6L, S7L |
| 9 | 9Vdc | S9U,S8U,S6U,S4U,S2U,S2L,S4L, S6L, S7L, S9L |
| 10 | 10Vdc | S11U,S10U,S8U,S6U,S4U,S2U,S2L, S4L,S6L,S8L,S9L |
| 11 | 11Vdc | S11U,S10U,S8U,S6U,S4U,S2U,S2L, S4L, S6L,S8L,S10L,S11L |
| 12 | 12Vdc | S13U,S12U,S10U,S8U,S6U,S4U, S2U, S2L, S4L,S6L,S8L,S10L,S11L |
| 13 | 13Vdc | S13U,S12U,S10U,S8U,S6U,S4U, S2U, S2L, S4L,S6L,S8L,S10L,S12L,S13L |
| 14 | 14Vdc | S14U,S12U,S10U,S8U,S6U,S4U, S2U, S2L, S4L,S6L,S8L,S10L,S12L,S13L |
| 15 | 15Vdc | S14U,S12U,S10U,S8U,S6U,S4U, S2U, S2L, S4L,S6L,S8L,S10L,S12L,S14L |
| 16 | 0 | T1 T3(or) T2 T4 |

Note: For symmetric topology, V1=V2=..=V15=Vdc
T1 and T4 is switched on for positive half cycle and T2 and T3 is switched on for negative half cycle.
The main disadvantage of this symmetric system is that, as the level increases, the size of the inverter also increases linearly. This in turn increases the conduction losses. It is observed that this

topology does not support asymmetrical source configuration.
C. Symmetric MLI by Menaka et.al in 2015
This symmetric topology proposed in [12] consist of two parts. The Single phase structure of a symmetric multilevel inverter is shown in Fig. 5. This inverter has two parts: one part is the level maker part which consists of separate dc sources (N) and main switches (N) and the other part is polarity maker part which consists of H-bridge cell. The separate dc sources(SDCS) used in this topology have the same magnitude equal to Vdc. H bridge is used to change the polarity of the output voltage in every half cycle and also produce the zero voltage level. The effective number of output phase voltage levels (Nlevel) in symmetric multilevel converter may be related to the number of separate dc sources (N) by Nlevel = 2N+1 and the number of switching devices is given by Nswitch = N+4. The maximum output voltage (Vo.max) of this proposed symmetric multilevel inverter is NVdc. Fig. 6 shows this topology for 31 level. The number of switches required for 31 level is nineteen only. The switches in the level maker part is subscripted from 1 to N and the switches in the polarity maker part is subscripted from A to D for simplicity. The switching states of this symmetric topology for 31 level is shown in the Table 3. Note: For symmetric topology,
V1=V2=..=V15=Vdc
SA and SB is switched on for positive half cycle and SC and SD is switched on for negative half cycle.

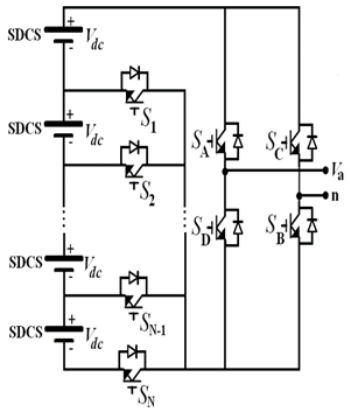


Fig. 5. Symmetric MLI by Menaka et.al in 2015

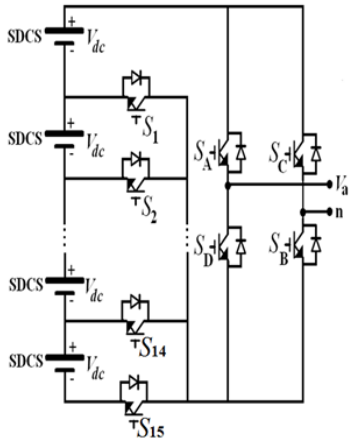


Fig. 6. Symmetric MLI by Menaka et.al in 2015

The main advantage of this topology is the lesser number of switches when compared to other symmetric topology. In this topology, equal load sharing amongst the input sources is not possible. However, one advantage offered by this MLI is that a total of three power electronic switches need to be conducting in all the switching states, thus resulting in lower conduction losses.

Table 3: Switching States of the Symmetric MLI proposed by Menaka et.al for 31 Level

| State | Output voltage | Switches in ON State |
|---|---|---|
| 1 | Vdc | S1 |
| 2 | 2Vdc | S2 |
| 3 | 3Vdc | S3 |
| 4 | 4Vdc | S4 |
| 5 | 5Vdc | S5 |
| 6 | 6Vdc | S6 |
| 7 | 7Vdc | S7 |
| 8 | 8Vdc | S8 |
| 9 | 9Vdc | S9 |
| 10 | 10Vdc | S10 |
| 11 | 11Vdc | S11 |
| 12 | 12Vdc | S12 |
| 13 | 13Vdc | S13 |
| 14 | 14Vdc | S14 |
| 15 | 15Vdc | S15 |
| 16 | 0 | SA,SD (or) SC,SB |

# 3 ASYMMETRIC TOPOLOGIES

In Asymmetric multilevel inverter topology, the magnitude of all dc voltage sources are different. Two topologies are discussed in the following section which are capable of working in asymmetrical topology.

A. Packed U Cell by Ounejjar et.al in 2008

Fig. 7 shows Packed U cell proposed in reference [13-17] for Nlevel. PUC topology has a simple structure with continuous U cell arrangement. Each U cell consist of two power switches and one input DC source. All the switches while conducting should be able to carry the load current.

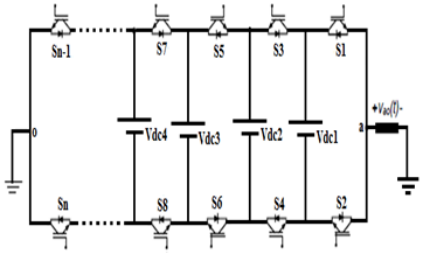


Fig. 7. Packed U Cell by Ounejjar et.al in 2008

The aforesaid topology for 31 level is shown in Fig. 8. It consist of ten IGBT switches and four DC sources. There are four U cells arranged together to produce 31 level output voltage. According to Youssef Ounejjar et al [16,17] this topology offers higher energy conversion efficiency. The structure due to its high compatibility requires very low production cost. The Table 4 shows the switching states of PUC inverter for 31 level. With a minimum of four DC sources and ten switches this topology is capable of producing 15 steps in the positive half and another 15 steps in the negative half cycle of the output waveform. In [17], the author has described about the topology with two sources. Even though the structure is simple, the control scheme is complex. It is observed that this topology does not support symmetrical source configuration.

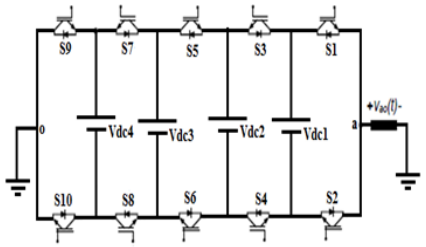


Fig. 8. Packed U Cell by Ounejjar et. al in 2008 for 31 level

Table 4: Switching States of PUC Inverter proposed by ounejjar et.al for 31 Level

| State | Output voltage *Vao(t)* | Switches in ON state |
|---|---|---|
| 1 | 0 | S1,S3,S5,S7,S9 |
| | 0 | S2,S4,S6,S8,S10 |
| 2 | Vdc1 | S1,S4,S6,S8,S10 |
| 3 | -Vdc1 | S2,S3,S5,S7,S9 |
| 4 | Vdc2 | S1,S3,S4,S6,S8 |
| 5 | -Vdc2 | S2,S4,S5,S7,S9 |
| 6 | Vdc3 | S1,S3,S5,S8,S10 |
| 7 | - Vdc3 | S2,S4,S6,S7,S9 |
| 8 | Vdc4 | S1,S3,S5,S7,S10 |
| 9 | - Vdc4 | S2,S4,S6,S8,S9 |
| 10 | Vdc4- Vdc3 | S2,S4,S6,S7,S10 |
| 11 | -(Vdc4- Vdc3) | S1,S3,S5,S8,S9 |
| 12 | Vdc3- Vdc2 | S2,S4,S5,S8,S10 |
| 13 | -(Vdc3- Vdc2) | S1,S3,S6,S7,S9 |
| 14 | Vdc4 - Vdc3 + Vdc2 | S2,S4,S5,S8,S9 |

| | | |
|---|---|---|
| 15 | -(Vdc4 -Vdc3 +Vdc2) | S1,S3,S6,S7,S10 |
| 16 | Vdc4-Vdc2 | S2,S4,S5,S7,S10 |
| 17 | -(Vdc4-Vdc2) | S1,S3,S6,S8,S9 |
| 18 | Vdc2-Vdc1 | S2,S3,S6,S8,S10 |
| 19 | -(Vdc2-Vdc1) | S1,S4,S5,S7,S9 |
| 20 | Vdc4-Vdc2+Vdc1 | S2,S3,S6,S8,S9 |
| 21 | - (Vdc4-Vdc2+Vdc1) | S1,S4,S5,S7,S10 |
| 22 | Vdc1-Vdc2+Vdc3-Vdc4 | S2,S3,S6,S7,S10 |
| 23 | -(Vdc1-Vdc2+Vdc3-Vdc4) | S1,S4,S5,S8,S9 |
| 24 | Vdc1-Vdc2+Vdc3 | S2,S3,S6,S7,S9 |
| 25 | -( Vdc1-Vdc2+Vdc3) | S1,S4,S5,S8,S10 |
| 26 | Vdc1-Vdc3 | S2,S3,S5,S8,S10 |
| 27 | -(Vdc1-Vdc3) | S1,S4,S6,S7,S9 |
| 28 | Vdc1-Vdc3+Vdc4 | S2,S3,S5,S8,S9 |
| 29 | -(Vdc1-Vdc3+Vdc4) | S1,S4,S6,S7,S10 |
| 30 | Vdc1-Vdc4 | S2,S3,S5,S7,S10 |
| 31 | -(Vdc1-Vdc4) | S1,S4,S6,S8,S9 |

B. Asymmetric Topology by Babaei et.al in 2015

In [18,19], Babaei et.al has proposed an optimal topology derived from the cascaded multilevel inverter. In this topology only unidirectional switches are used. The Fig. 9 shows the general asymmetric topology for Nlevel. It consists of 2n dc voltage sources (n is the number of dc voltage sources on each leg) and 4n+2 power switches for Nlevel (22n+1 - 1). In [18,19], the authors have also proposed two algorithms to generate the positive and negative voltage levels at the output. This topology includes the H-bridge structure within the main structure instead of keeping it separately thus minimizing the usage of two switches. Also in [18], authors have compared many new topologies with reduced device count are with their newly proposed topology. The maximum output voltage (Vo.max) of this asymmetric multilevel inverter is VLn + VRn. The Fig. 10 shows the asymmetric topology proposed by Babaei et al for 31 level. In this topology the values of DC voltage sources should be different to generate more voltage levels. This helps in the usage of less num-

ber of switches and DC voltage sources for producing higher levels. According to the authors if the values of the DC voltage sources are equal, the number of voltage levels decreases to three.

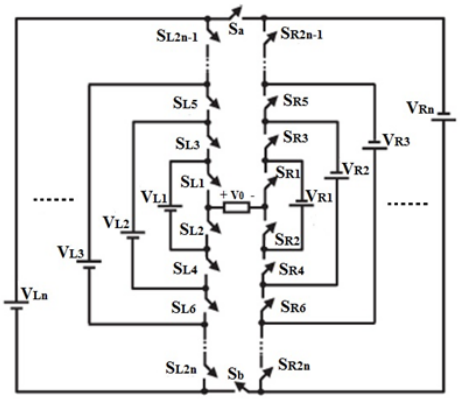


Fig. 9. Asymmetric MLI Topology by Babaei et.al in 2015

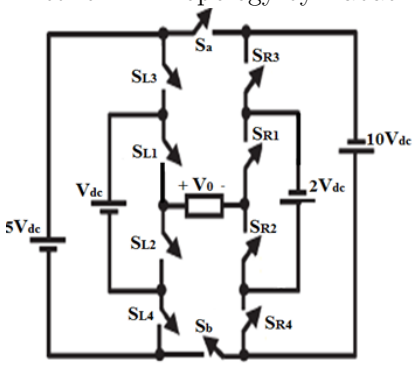


Fig. 10. Asymmetric MLI Topology by Babaei et.al in 2015 for 31.level

The simultaneous switching ON of switches Sa and Sb should be avoided. It is to be noted that the DC sources connected on either sides have different polarity. Only ten switches and four DC sources are required for 31 level inverter. Since DC voltage sources of low magnitude are needed, the cost of this inverter is considerably less. Table 5 shows the switching sequences of the inverter for 31 level configuration. A minimum of five switches are conducting for a single level. The compact size and minimal use of the components in

the topology makes it the optimal one among the recently proposed topologies with reduced device count.

Table 5: Switching States of Asymmetric MLI proposed by Babaei et.al for 31 Level

| State | Output voltage | Switches in ON State |
|---|---|---|
| 1 | 15 Vdc | SL1,SL3,SR1,SR3,Sb |
| 2 | 14 Vdc | SL2,SL3,SR1,SR3,Sb |
| 3 | 13 Vdc | SL1,SL3,SR2,SR3,Sb |
| 4 | 12 Vdc | SL2,SL3,SR2,SR3,Sb |
| 5 | 11 Vdc | SL1,SL4,SR1,SR3,Sb |
| 6 | 10 Vdc | SL2,SL4,SR1,SR3,Sb |
| 7 | 9 Vdc | SL1,SL4,SR2,SR3,Sb |
| 8 | 8 Vdc | SL2,SL4,SR2,SR3,Sb |
| 9 | 7 Vdc | SL1,SL3,SR1,SR4,Sb |
| 10 | 6 Vdc | SL2,SL3,SR1,SR4,Sb |
| 11 | 5 Vdc | SL1,SL3,SR2,SR4,Sb |
| 12 | 4 Vdc | SL2,SL3,SR2,SR4,Sb |
| 13 | 3 Vdc | SL1,SL4,SR1,SR4,Sb |
| 14 | 2 Vdc | SL2,SL4,SR1,SR4,Sb |
| 15 | Vdc | SL1,SL4,SR2,SR4,Sb |
| 16 | 0 | SL2,SL4,SR2,SR4,Sb |

# 4 SYMMETRIC AND ASYMMETRIC TOPOLOGIES

In this section some of the multilevel inverters with reduced device count that are applicable for both symmetric as well as asymmetric topologies are discussed. These inverters therefore can have either equal or different magnitude of input DC voltage sources.

A. MLI by Hinago and Koizumi in 2010

The single phase multilevel inverter proposed by Hinago and Koizumi in [25,26] consist of DC sources and H-bridge that can be switched in series and in parallel. According to the authors the inverter can be applied in electric vehicle. The power requirement of a vehicle can be met by different combinations of series or parallel connections. Fig. 11 shows the MLI for Nlevel for both symmetric and asymmetric topology.

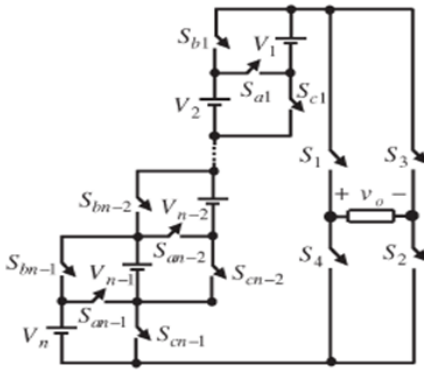


Fig. 11. MLI by Hinago and Koizumi in 2010 for Nlevel

Symmetric topology Authors of literature, [25,26] have explained about the symmetric topology with four DC sources. According to the authors, the limitation in this topology is that the switches with higher blocking capability cannot be operated at fundamental switching frequency. Fig. 12 shows the aforesaid topology for 31 level. A total of forty six switches and fifteen DC sources are essential for 31 level output. Among these forty two switches are used for level creating part and the rest is for H-bridge or the polarity generation part. The voltage levels which can be synthesized by the switched sources part are summarized in Table 6. From the table it can be inferred that with input sources of equal voltages, equal load sharing is possible amongst them. In this multilevel inverter all additive configurations are possible. Note: For symmetric topology,
V1=V2=..=V15=Vdc
T1 and T4 is switched on for positive half cycle and T2 and T3 is switched on for negative half cycle.

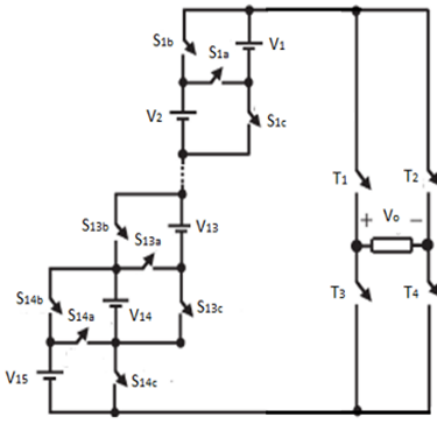


Fig. 12. MLI by Hinago and Koizumi in 2010 for 31 level (Symmetric topology)

Table 6: Switching States of MLI proposed by Hinago and Koizumi for 31 Level (Symmetric topology)

| State | Output voltage | Switches in ON State |
|---|---|---|
| 1 | Vdc | S1c,S2c,S3c,S4c,S5c,S6c,S7c,S8c, S9c, S10c,S11c,S12c,S13c,S14c |
| 2 | 2Vdc | S1a,S2c,S3c,S4c,S5c,S6c,S7c,S8c, S9c, S10c,S11c,S12c,S13c,S14c |
| 3 | 3Vdc | S1a,S2a,S3c,S4c,S5c,S6c,S7c,S8c, S9c, S10c,S11c,S12c,S13c,S14c |
| 4 | 4Vdc | S1a,S2a,S3a,S4c,S5c,S6c,S7c,S8c, S9c, S10c,S11c,S12c,S13c,S14c |
| 5 | 5Vdc | S1a,S2a,S3a,S4a,S5c,S6c,S7c,S8c, S9c, S10c,S11c,S12c,S13c,S14c |
| 6 | 6Vdc | S1a,S2a,S3a,S4a,S5a,S6c,S7c,S8c, S9c, S10c,S11c,S12c,S13c,S14c |
| 7 | 7Vdc | S1a,S2a,S3a,S4a,S5a,S6a,S7c,S8c, S9c, S10c,S11c,S12c,S13c,S14c |
| 8 | 8Vdc | S1a,S2a,S3a,S4a,S5a,S6a,S7a,S8c, S9c, S10c,S11c,S12c,S13c,S14c |
| 9 | 9Vdc | S1a,S2a,S3a,S4a,S5a,S6a,S7a,S8a, S9c, S10c,S11c,S12c,S13c,S14c |
| 10 | 10Vdc | S1a,S2a,S3a,S4a,S5a,S6a,S7a,S8a, S9a, S10c,S11c,S12c,S13c,S14c |
| 11 | 11Vdc | S1a,S2a,S3a,S4a,S5a,S6a,S7a,S8a, S9a, S10a,S11c,S12c,S13c,S14c |
| 12 | 12Vdc | S1a,S2a,S3a,S4a,S5a,S6a,S7a,S8a, S9a, S10a,S11a,S12c,S13c,S14c |
| 13 | 13Vdc | S1a,S2a,S3a,S4a,S5a,S6a,S7a,S8a, S9a, S10a,S11a,S12a,S13c,S14c |
| 14 | 14Vdc | S1a,S2a,S3a,S4a,S5a,S6a,S7a,S8a, S9a, S10a,S11a,S12a,S13a,S14c |
| 15 | 15Vdc | S1a,S2a,S3a,S4a,S5a,S6a,S7a,S8a, S9a, S10a,S11a,S12a,S13a,S14a |
| 16 | 0 | T1T3 (OR) T2T4 |

Asymmetric topology In [25,26],authors do not comment on the asymmetric source configuration but the topology enables the possibility of all additive combinations.

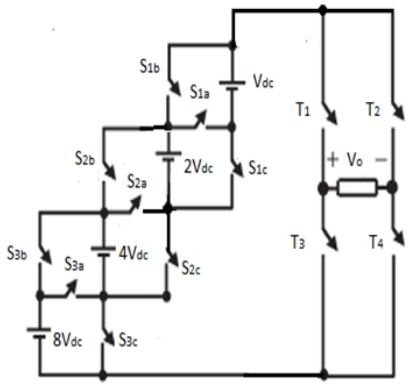


Fig. 13. MLI by Hinago and Koizumi in 2010 for 31 level (Asymmetric topology)

Fig. 13 shows the switched series/parallel sources based MLI for 31 level asymmetric topology. As similar to the previous topology this MLI also consist of level generation part and polarity generation part. The switching states for this topology can be observed from the Table 7. T1 and T4 is switched on for positive half cycle and T2 and T3 is switched on for negative half cycle.

Table 7: Switching States of MLI proposed by Hinago and Koizumi for 31 Level (Asymmetric topology)

| State | Output voltage | Switches in ON State |
|---|---|---|
| 1 | Vdc | S1c,S2c,S3c |
| 2 | 2Vdc | S1b,S2c,S3c |
| 3 | 3Vdc | S1a,S2c,S3c |
| 4 | 4Vdc | S1b,S2b,S3c |
| 5 | 5Vdc | S1a,S2b,S3c |
| 6 | 6Vdc | S1b,S2a,S3c |
| 7 | 7Vdc | S1a,S2a,S3c |
| 8 | 8Vdc | S1b,S2b,S3b |
| 9 | 9Vdc | S1a,S2b,S3b |
| 10 | 10Vdc | S1b,S2a,S3b |
| 11 | 11Vdc | S1a,S2a,S3b |
| 12 | 12Vdc | S1b,S2b,S3a |
| 13 | 13Vdc | S1a,S2b,S3a |
| 14 | 14Vdc | S1b,S2a,S3a |
| 15 | 15Vdc | S1a,S2a,S3a |
| 16 | 0 | T1T3 (OR) T2T4 |

B. Multilevel DC Link Inverter (MLDCL) by Gui Jia su in 2004
In [27,28], Gui Jia Su has proposed a modified cascaded H-bridge based multilevel inverter which is referred to as MLDCL inverter. Compared to the classical cascaded topology MLDCL is more advantageous due to its reduced device count. MLDCL inverter for Nlevel is shown in Fig. 14. In his paper the author describes about the symmetric topology for MLDCL inverter. In this section both symmetric and asymmetric topologies for 31 level are discussed.
Symmetric topology Symmetric topology of MLDCL inverter is shown in Fig. 15. It can be observed that the polarity generation part must have a minimum voltage blocking capability equal to the sum of the input voltage sources.
Note: For symmetric topology,
V1=V2=..=V15=Vdc
T1 and T4 is switched on for positive half cycle and T2 and T3 is switched on for negative half cycle.

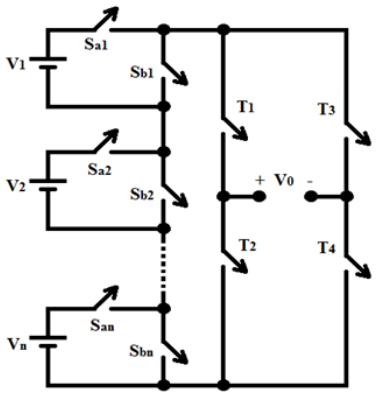


Fig. 14. MLDCL Inverter by for Nlevel

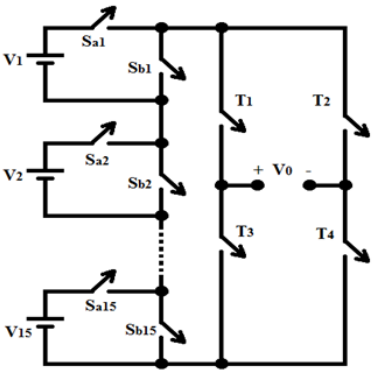


Fig. 15. MLDCL Inverter for 31 level (Symmetric topology)

From the Table 8 it is clear that many switches are in the conducting state for all the voltage levels. Thus switches can be eliminated permanently and thus reduce the number of switches used. The main drawback is that for a 31 level topology, a total of sixteen switches have to conduct to generate the required output voltage which further increases for higher levels.

Asymmetric topology In asymmetric topology for MLDCL, subtractive combinations of the input DC levels cannot be synthesized. This in turn do not allow any trinary source configuration. A 31 level asymmetric topology for MLDCL inverter is shown in Fig. 16.The total number of switches required for asymmetric MLDCL topology is given by [( Nlevel+1)/4 +4] .Thus for a 31 level MLDCL twelve power switches are required. The number of DC voltage sources required is given by (Nlevel+1)/8. Hence the sources re-

quired is four.

Table 8: Switching States of MLDCL Topology proposed by Gui Jia Su for 31 Level (Symmetric topology)

| State | Output voltage | Switches in ON State |
|---|---|---|
| 1 | Vdc | Sa1,Sb2,Sb3,Sb4,Sb5,Sb6,Sb7,Sb8, Sb9,Sb10,Sb11,Sb12,Sb13,Sb14,Sb15 |
| 2 | 2Vdc | Sa1,Sa2,Sb3,Sb4,Sb5,Sb6,Sb7,Sb8, Sb9,Sb10,Sb11,Sb12,Sb13,Sb14,Sb15 |
| 3 | 3Vdc | Sa1,Sa2,Sa3,Sb4,Sb5,Sb6,Sb7,Sb8, Sb9,Sb10,Sb11,Sb12,Sb13,Sb14,Sb15 |
| 4 | 4Vdc | Sa1,Sa2,Sa3,Sa4,Sb5,Sb6,Sb7,Sb8, Sb9,Sb10,Sb11,Sb12,Sb13,Sb14,Sb15 |
| 5 | 5Vdc | Sa1,Sa2,Sa3,Sa4,Sa5,Sb6,Sb7,Sb8, Sb9,Sb10,Sb11,Sb12,Sb13,Sb14,Sb15 |
| 6 | 6Vdc | Sa1,Sa2,Sa3,Sa4,Sa5,Sa6,Sb7,Sb8, Sb9,Sb10,Sb11,Sb12,Sb13,Sb14,Sb15 |
| 7 | 7Vdc | Sa1,Sa2,Sa3,Sa4,Sa5,Sa6,Sa7,Sb8, Sb9,Sb10,Sb11,Sb12,Sb13,Sb14,Sb15 |
| 8 | 8Vdc | Sa1,Sa2,Sa3,Sa4,Sa5,Sa6,Sa7,Sa8, Sb9,Sb10,Sb11,Sb12,Sb13,Sb14,Sb15 |
| 9 | 9Vdc | Sa1,Sa2,Sa3,Sa4,Sa5,Sa6,Sa7,Sa8, Sa9,Sb10,Sb11,Sb12,Sb13,Sb14,Sb15 |
| 10 | 10Vdc | Sa1,Sa2,Sa3,Sa4,Sa5,Sa6,Sa7,Sa8, Sa9,Sa10,Sb11,Sb12,Sb13,Sb14,Sb15 |
| 11 | 11Vdc | Sa1,Sa2,Sa3,Sa4,Sa5,Sa6,Sa7,Sa8, Sa9,Sa10,Sa11,Sb12,Sb13,Sb14,Sb15 |
| 12 | 12Vdc | Sa1,Sa2,Sa3,Sa4,Sa5,Sa6,Sa7,Sa8, Sa9,Sa10,Sa11,Sa12,Sb13,Sb14,Sb15 |
| 13 | 13Vdc | Sa1,Sa2,Sa3,Sa4,Sa5,Sa6,Sa7,Sa8, Sa9,Sa10,Sa11,Sa12,Sa13,Sb14,Sb15 |
| 14 | 14Vdc | Sa1,Sa2,Sa3,Sa4,Sa5,Sa6,Sa7,Sa8, Sa9,Sa10,Sa11,Sa12,Sa13,Sa14,Sb15 |
| 15 | 15Vdc | Sa1,Sa2,Sa3,Sa4,Sa5,Sa6,Sa7,Sa8, Sa9,Sa10,Sa11,Sa12,Sa13,Sa14,Sa15 |
| 16 | 0 | T1,T3 (or) T2,T4 |

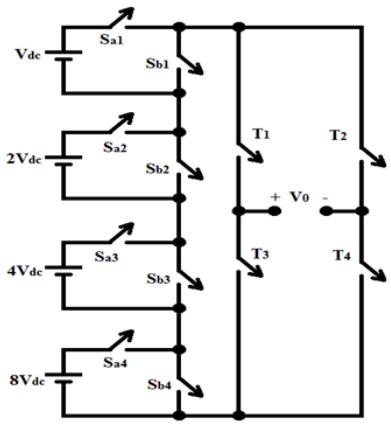


Fig. 16.MLDCL Inverter for 31 level (Asymmetric topology)

Table 9: Switching States of MLDCL proposed by Gui Jia Su for 31 Level (Asymmetric topology)

| State | Output voltage | Switches in ON State |
|---|---|---|
| 1 | Vdc | Sa1,Sb2,Sb3,Sb4 |
| 2 | 2Vdc | Sb1,Sa2,Sb3,Sb4 |
| 3 | 3Vdc | Sa1,Sa2,Sb3,Sb4 |
| 4 | 4Vdc | Sb1,Sb2,Sa3,Sb4 |
| 5 | 5Vdc | Sa1,Sb2,Sa3,Sb4 |
| 6 | 6Vdc | Sb1,Sa2,Sa3,Sb4 |
| 7 | 7Vdc | Sa1,Sa2,Sa3,Sb4 |
| 8 | 8Vdc | Sb1,Sb2,Sb3,Sa4 |
| 9 | 9Vdc | Sa1,Sb2,Sb3,Sa4 |
| 10 | 10Vdc | Sb1,Sa2,Sb3,Sa4 |
| 11 | 11Vdc | Sa1,Sa2,Sb3,Sa4 |
| 12 | 12Vdc | Sb1,Sb2,Sa3,Sa4 |
| 13 | 13Vdc | Sa1,Sb2,Sa3,Sa4 |
| 14 | 14Vdc | Sb1,Sa2,Sa3,Sa4 |
| 15 | 15Vdc | Sa1,Sa2,Sa3,Sa4 |
| 16 | 0 | T1,T3 (or) T2,T4 |

Note: T1 and T4 is switched on for positive half cycle and T2 and T3 is switched on for negative half cycle.
Author suggests the application of permanent magnet motor drives with MLDCL inverter. It can also be applied in distributed power generation involving fuel cells and photovoltaic cells. C. Classical cascaded multilevel inverter

As many of the multilevel inverters proposed now a days are derived from classical cascaded inverter [31], its comparison with those newly proposed is found to be essential. This basic topology consist of series connected H-bridges supplied from several DC sources. Fig. 17 shows the aforesaid topology for Nlevel. Each H-bridge unit generates a quasi square waveform by phase shifting its positive and negative phase-leg-switching timings.

Symmetric topology For a classical cascaded topology symmetric configuration produces a bulky structure with fifteen H-bridges. The topology consist of fifteen DC voltage sources and hence the same number of H-bridges. Fig. 18 shows the aforesaid topology for 31 level symmetric configuration. The absence of separate polarity generation H-bridge makes the circuit complicated. Both the level and the polarity generation are completed in the H-bridges. The switching sequences of the switches are described in the Table 10.

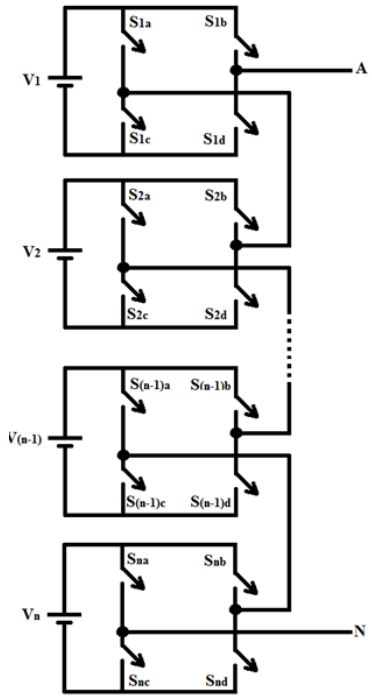


Fig. 17.Classical cascaded topology for Nlevel

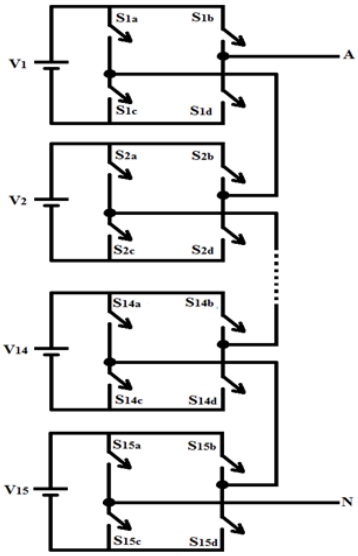


Fig. 18.Classical cascaded topology for 31 level (Symmetric Topology)

Table 10: Switching States of classical cascaded MLI (Symmetric topology)

| State | Output voltage | Switches in ON State |
|---|---|---|
| 1 | Vdc | S1a,S1d |
| 2 | 2Vdc | S1a,S1d,S2a,S2d |
| 3 | 3Vdc | S1a,S1d,S2a,S2d,S3a,S3d |
| … | … | …… |
| 13 | 13Vdc | S1a,S1d,S2a,S2d,…… S13a,S13d |
| 14 | 14Vdc | S1a,S1d,S2a,S2d,…… S14a,S14d |
| 15 | 15Vdc | S1a,S1d,S2a,S2d,…… S15a,S15d |
| 16 | 0 | Any two switches on the same leg |
| 17 | -Vdc | S1b,S1c |
| 18 | -2Vdc | S1b,S1c,S2b,S2c |
| 19 | -3Vdc | S1b,S1c,S2b,S2c,S3b,S3c |
| … | … | …. |
| 29 | -13Vdc | S1b,S1c,S2b,S2c,…… S13b,S13c |
| 30 | -14Vdc | S1b,S1c,S2b,S2c,…… S14b,S14c |
| 31 | -15Vdc | S1b,S1c,S2b,S2c,…… S15b,S15c |

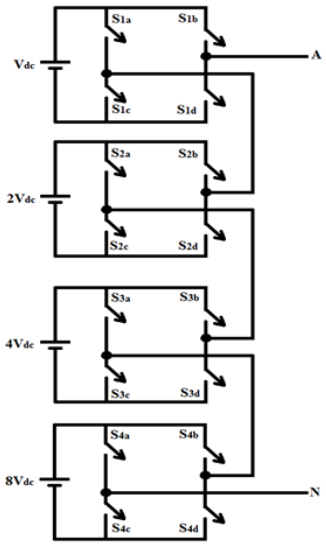


Fig. 19. Classical cascaded topology for 31 level(Asymmetric topology)

Asymmetric topology Fig. 19 shows the cascaded topology for 31 level asymmetric configuration. A total of (Nlevel+1)/2 switching devices are required for this topology. It is to be noted that each switching device always conducts for a half cycle and this makes switching devices to share the current stresses equally. For a 31 level asymmetric configuration a total of four DC sources and sixteen switches are needed. In classical cascaded topology, there is no level generating part and polarity generation part as observed in new proposed topologies. Table 11 shows the switching states of the classical cascaded topology.

Table 11: Switching States of classical cascaded MLI (Asymmetric topology)

| State | Output voltage | Switches in ON State |
|---|---|---|
| 1 | Vdc | S1a,S1d |
| 2 | 2Vdc | S2a,S2d |
| 3 | 3Vdc | S1a,S1d, S2a,S2d |
| 4 | 4Vdc | S3a,S3d |
| … | … | …. |
| 12 | 12Vdc | S3a,S3d, S4a,S4d |
| 13 | 13Vdc | S1a,S1d, S3a,S3d, S4a,S4d |
| 14 | 14Vdc | S2a,S2d, S3a,S3d, S4a,S4d |
| 15 | 15Vdc | S1a,S1d, S2a,S2d, S3a,S3d, S4a,S4d |
| 16 | 0 | Any two switches on the same leg |
| 17 | -Vdc | S1b,S1c |
| 18 | -2Vdc | S2b,S2c |
| 19 | -3Vdc | S1b,S1c, S2b,S2c |
| 20 | -4Vdc | S3b,S3c |
| … | … | ….. |
| 28 | -12Vdc | S3b,S3c, S4b,S4c |
| 29 | -13Vdc | S1b,S1c, S3b,S3c, S4b,S4c |
| 30 | -14Vdc | S2b,S2c, S3b,S3c, S4b,S4c |
| 31 | -15Vdc | S1b,S1c, S2b,S2c, S3b,S3c, S4b,S4c |

# 5 DISCUSSIONS

From the analysis of previous section, the performance of the different symmetric and asymmetric topologies can be commented. The topologies discussed in symmetric configuration are not suitable for asymmetric mode of operation and vice-versa. In the discussion of the topologies for both symmetric and asymmetric configuration, two major recently proposed topologies with reduced device count

are compared with the classical cascaded topology to recognize the large reduction in switches and increased quality of the latest over the basic. Among them the recently proposed topology by Babaei in 2015 shows the optimized model for an MLI. According to the availability of independent DC sources it can be used accordingly. The configuration has the similar compact size as that of Packed U cell configuration which is only applicable to asymmetric topology. Symmetric topology proposed by menaka in 2015 has more advantageous over other symmetric topology. It is also observed from the previous section that the number of switches that conduct current for higher levels are considerably large. This increases the necessity of large number of switches for higher levels. Many topologies require the utilization of bidirectional switches which should be considered while its design. The topologies with separate H-bridges for polarity generation imparts much stress on these switches to carry the total input voltage.

ADVANTAGES AND DISADVANTAGES OF MULTILEVEL INVERTER TOPOLOGIES WITH REDUCED DEVICE COUNT

| TOPOLOGY | REFERENCE | ADVANTAGES | DISADVANTAGES |
|---|---|---|---|
| H-bridge based MLI by Choi and Kang in 2009 | [5,6] | • Increase in level possible easily | • Stresses on the switches are high |
| Symmetric MLI by Babaei et.al in 2012 | [9,10,11] | • Many possible ways for generation of a single level<br>• Better performance | • Switches used are bidirectional |
| Symmetric MLI by Menaka et.al in 2015 | [12] | • Simple Structure<br>• Less Conduction Losses | • equal load sharing among the input sources is not possible |
| Packed U-Cell (PUC) by Ounejjar et.al in 2008 | [13-17] | • Less losses<br>• Simple structure | • Complex control<br>• Isolated input DC levels are required |
| Asymmetric MLI by Babaei et.al in 2015 | [18,19] | • Compact structure<br>• Optimum utilization of the components<br>• Bidirectional switches are not used<br>• Higher levels with less number of DC sources | • Different values of DC sources are used.<br>• High quality switches should be used |
| MLI by Hinago and Koizumi in 2010 | [25,26] | • Equal load sharing is possible<br>• Applicable for both symmetric and asymmetric configurations | • Increasing the level needs great care |
| Multilevel DC Link Topology | [27,28] | • Simple structure<br>• Symmetric configuration is compact in structure. | • In asymmetric configuration a large number of switches under conduction |
| Classical cascaded Topology | [31] | • Simple structure to understand the concepts<br>• Increase in level possible easily<br>• No separate H –bridges are used | • Complex and large structure<br>• Switching losses are high<br>• High device count |

In the previous table, advantages and limitations of the topologies are commented on the basis of which the correct choice for different applications can be made. This helps in calculating the overall cost as well as the performances of different topologies can be derived at. Since all the topologies are compared for 31 level they can also be discussed for the usage in three phase applications.

# 6 CONCLUSION

Multilevel Inverters with reduced device counts are paving the way for researchers to derive and propose highly accurate solutions for the various applications in power system. Thus the choice of inverters plays a major role in performance of the entire system. The comparison made in this paper will facilitate the readers to choose the better option for the requirement. The three major classifications of the topologies (symmetric, asymmetric, both symmetric and asymmetric) in this paper gives a clarified image of the topologies. By this classification and comparison, the different challenges and compromises that are made while reducing the device count are also reviewed. In addition, the paper creates an updated view of the recent developments in this field.

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