Design and Analysis of Interleaved SEPIC converter

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Abstract*—This paper presents the design and analysis of High gain Interleaved Single Ended Primary Inductor Converter (SEPIC) for renewable energy applications. Simulations are carried out using MATLAB Simulink. Interleaved SEPIC converter operates under both continuous and discontinuous modes of operations. Interleaved SEPIC's output voltage is greater than or less than or equal to its input voltage. By using interleaved method, the converter's switching stress is reduced and efficiency is also increased. To maintain a constant output voltage instead of changing voltage, closed loop control is required. This converter has low switch voltage and high efficiency. It is used for low input voltage and high-power applications. This paper gives design and analysis of Interleaved SEPIC converter for an Input voltage of 24V, output voltage of 48V with output power of 100W.

Keywords: DC-DC converter, High gain Interleaved SEPIC.

I. INTRODUCTION

Due to proliferation in electricity power demand and also increase in renewable energy sources, renewable energy sources are mostly used in the electric power generation to meet out the demand. The renewable energy sources are used in residential appliances and grid connected systems. The renewable energy sources are low voltages. In order to increase the voltage or high-power applications it is necessary to boost up the voltage by using power converters. In this converter act as a voltage-double circuit in terms of renewable sources. The converters are classified into two types namely, isolated and non-isolated converters. The isolated step up converters have a transformer and by varying the turns ratio of the transformer, high voltage gain can be achieved. Some of those converters are fly back, push-pull, and forward type convert etc. [1-2]. The fly back converter has a drawback of high voltage stress due to transformer leakage inductances which reduce the efficiency [3]. Among non-isolated converter family, the classical boost converter generates the high step-up voltage gain by using large duty cycle. This may cause the high switching voltage stress with reverse recovery issues and reduce the high step up conversion efficiency and also system goes to unstable state. The high step-up converter efficiency is improved by using coupled inductor [4-5], which generates high voltage gain, by adjusting the turns ratio of coupled inductor similar to isolated converters. However, the main switch is affected by voltage stress and high voltage spike due to the leakage inductance of coupled inductor. Due to this leakage, the overall conversion efficiency gets reduced. In literature, to overcome the above demerits, active and passive clamping strategies have been adopted [6]with coupled inductor, which also increases the cost and size of converters. Some high step-up converters are developed by combining two converters so as to achieve the high voltage gain, namely: classical boost converter combines with single ended primary inductor converter (SEPIC)[7,8]and boost with cuk [9]. These converters have the switching voltage equal to the average sum of input and output voltage. The integrated fly back with boost converter is proposed in [10-11] where the coupled inductor is considered as a fly back converter. The dissipated energy from the leakage inductor is recycled by the load, and it limits the main switching voltage stress. Interleaved boost converter is used to reduce the input ripple current and it doubles the transferable power [12-13]. But the controlling of switches becomes complex and exhibits low conversion efficiency for high voltage applications. To overcome the above drawbacks, this paper proposes a non-isolated high step up converter to generate high voltage gain using interleaved converter. The proposed converter topology utilizes a interleaving in the SEPIC converter. The advantages of this converter are high voltage conversion, low conduction loss, low voltage stress across the semiconductor devices, fewer components and is easy to control. Interleaved SEPIC converter operates on both CCM and DCM modes of operations.

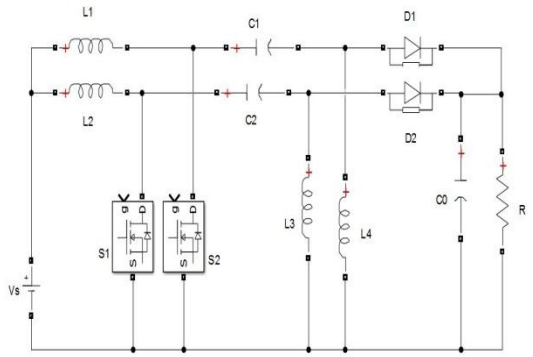

Fig.1 Non-isolated DC-DC converter

II. CIRCUIT CONFIGURATION

The circuit diagram of the non-isolated DC-DC converter is shown in Fig.1. The circuit consists of switch S_1 and S_2, inductors L_1,L_2,L_3, and L_4, Capacitor C_1,C_2& diodes D_1,D_2. Compare with the conventional SEPIC converter, instead of using single switch, two switches are used in this converter. It may lead to improve the high voltage gain and also the efficiency and reduces the switching stress. The capacitor C_2 is energized same as to the conventional boost converter.

A. Operating Principle:

The Continuous Conduction Mode (CCM) of the non-isolated Dc-DC converter is working on four modes of operation is shown in fig 2,3,4 and 5.

Mode1: Both S1 and S2 are ON

Inductor L1 remains in Imin1 level, L2 remains in Imax1 and L3 remains in Imin2, L4 remains in Imax2 during this period. Capacitor C2 and C3 supply L2 and L4 respectively. Output Capacitor discharges and supplies the load Current to the load is continuous.

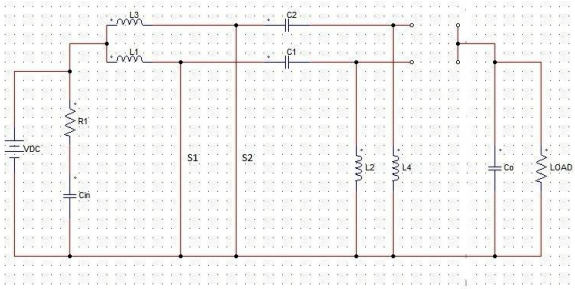

Fig.2. Mode-1 of operation.

Mode2: S1 OFF and S2 ON

Inductor L1 de-energizes to Imin1 and C1 gets charged. The inductor L4 supplies the output capacitor C0 and the load through diode D2. The inductor L2 is energized to Imax1. Inductor L3 energizes to level Imax2 and L2 is energized to level Imax2 during this period.

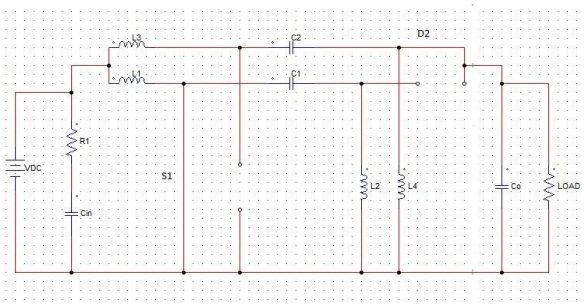

Fig.3. Mode-2of operation.

Mode-3:S1 ON and S2 OFF

Inductor L4 de-energizes to Imin2 and C2 gets charged. The inductor L2 supplies the output capacitor C0 and the load through diode D1. The inductor L1 is energized to Imax1. Inductor L3 energizes to level Imax2 and L2 is de-energized to level Imin2 during this period.

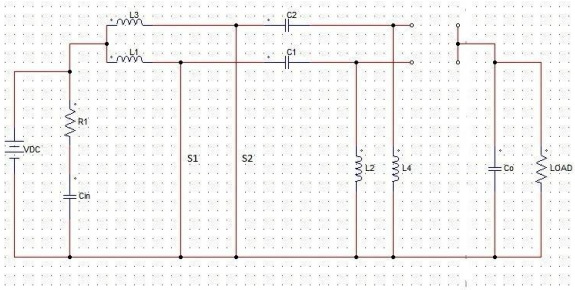

Fig.4. Mode-3of operation.

Mode-4:Both S1 and S2 OFF

L1 de-energizes and C1 gets charged. L2 supplies output capacitor and the load through diode D2. Similarly, L3 de-energizes and C2 gets charged. L4 supplies the output capacitor and the load through D1.

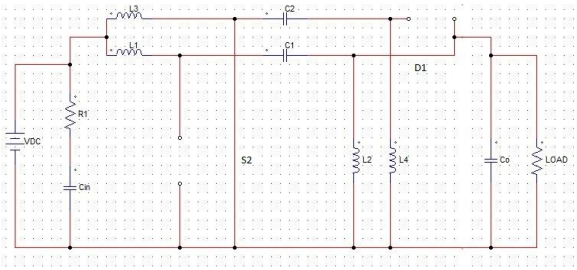

Fig.5. Mode-4of operation.

The main theoretical waveforms for the proposed converter topology under CCM are shown in fig.6.

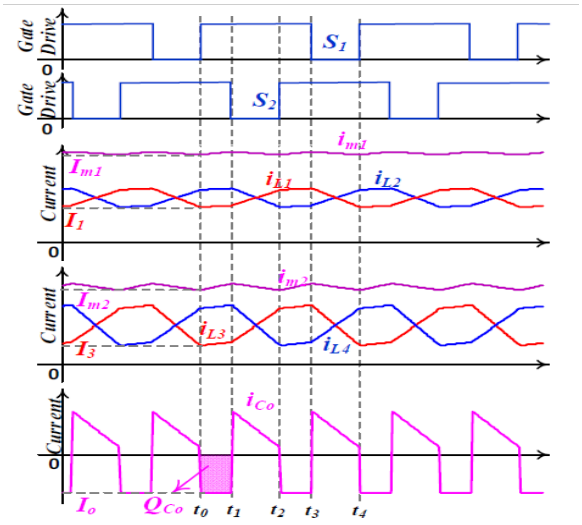

Fig.6. Theoretical waveforms for CCM

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III. DESIGN OF INTERLEAVED SEPIC CONVERTER

The Interleaved SEPIC converter operates in Continuous Conduction Mode at a rating of the 100W and is designed by the following specifications. The output Voltage (V_{out}) of the converter is 48V and theinput voltage (V_{in}) is 24V. switching frequency of the converter is 20 kHz and duty cycle is 66%.

Design of the Interleaved SEPIC is done by the following equations are mentioned here.

The voltage relationship is given by

$$V_o = V_{in}(D)/(1-D)(1)$$

where D = Duty cycle

V_0 = Output Voltage

V_{in} = Input Voltage

The following Table I represents the design parameters of the Interleaved SEPIC converter

TABLE I Design Specifications of Interleaved SEPIC converter

PARAMETERS	VALUES
Input voltage	24V
Output Voltage	48 V
Switching Frequency	20 kHZ
Duty Cycle (α)	66%
Inductance(L) L_1& L_2	162µH & 142.85µH
Capacitance (C) C_1,C_2&C_0	2.75µF & 0.468 mF
Resistor	23.04Ω

IV.SIMULATION OF INTERLEAVED SEPIC CONVERTER

fig.7. shows the Simulink diagram of the Interleaved SEPIC converter that is supplied by DC source of 24V and it produces the output of 230V with L and C values as in TABLE I

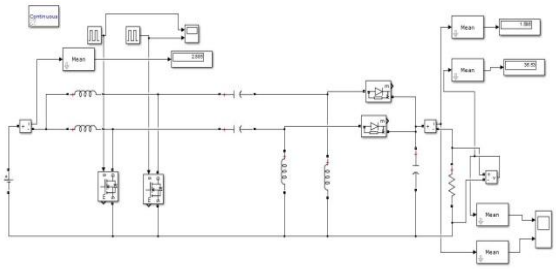

Fig.7. Simulation diagram for open loop operation of Interleaved SEPIC converter

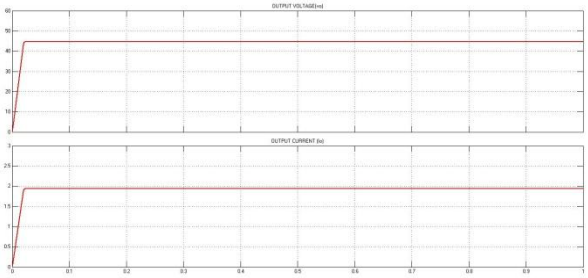

Fig.8. Open loop response of Interleaved SEPIC converter

The Output voltage response of the converter is shown in Fig.8. From the output voltage waveform, it is inferred that, the desired output voltage is not achieved, hence a closed loop controller is needed.

fig.9. shows the closed loop Simulink diagram of the Interleaved SEPIC converter that is supplied by DC source of 24V and it produces an output of 48V.

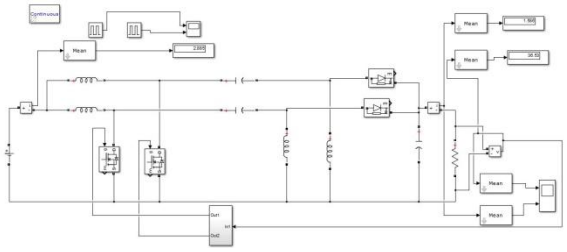

Fig.9. Simulation diagram of closed loop operation of Interleaved SEPIC converter.

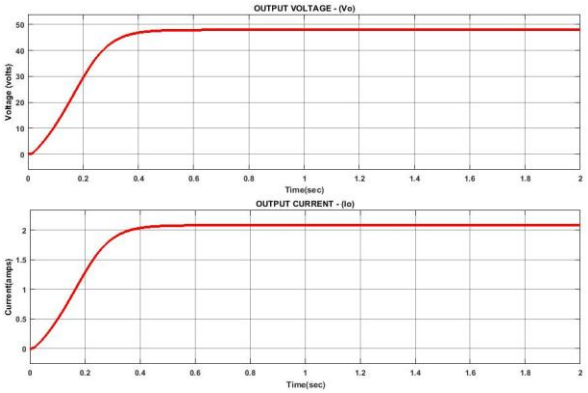

Fig.10. Closed loop response of Interleaved SEPIC converter

From the closed loop output voltage waveform, it is inferred that, there is zero peak overshoot and settling time is also less and the desired output voltage is obtained. From the closed loop current waveform, it is inferred that, similar to the output voltage waveform because of resistive load.

V. ANALYSIS OF Interleaved SEPIC CONVERTER

In order to scrutinize the effectiveness of the Interleaved SEPIC converter the simulation analysis is given below.

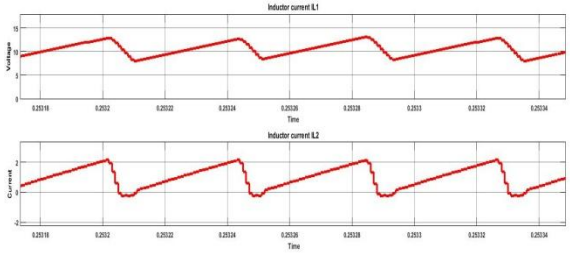

Fig.11. Inductor Current response of interleaved SEPIC converter

From fig.11.which shows inductor current waveform, it is inferred that, inductor current is above zero and there is no zero crossing in the inductor current waveform this converter operates under CCM.

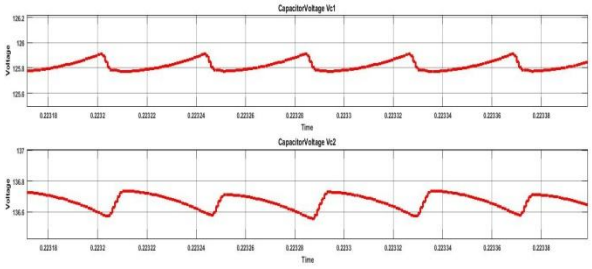

Fig.12. capacitor voltage response of Interleaved SEPIC converter

From fig.12, it is inferred that, the sum of the capacitors C1 and C2 voltage is equal to the output voltage of the converter.

TABLE II VARIATION IN SUPPLY VOLTAGE

S. NO	V_S(V)	I_s(A)	V_o(V)	I_o(A)	η
1	20	3.613	39.20	1.702	92.33
2	24	4.350	47.20	2.049	92.64
3	48	8.770	95.19	4.132	93.44

TABLE II shows the open loop variation in supply voltage.

TABLE III VARIATION IN DUTY CYCLE

S. NO	V_S(V)	I_s(A)	D	V_o(V)	I_o(A)	η
1	24	0.021	0.1	1.864	0.081	29.924
2	24	0.081	0.2	5.191	0.225	60.161
3	24	0.217	0.3	9.466	0.411	74.667
4	24	0.503	0.4	15.160	0.658	82.603
5	24	1.098	0.5	23.090	1.002	87.797
6	24	5.702	0.6	54.160	2.351	93.045
7	24	16.140	0.7	90.880	3.944	92.532

TABLE III shows the variation in Duty cycle. It is inferred that, when the Duty cycle of the converter is varied its output voltage also changes correspondingly.

TABLE IV VARIATION IN LOAD RESISTANCE

S.NO	V_S(V)	I_S(A)	%LOAD (Ω)	V_O (V)	I_O(A)	η
1	24	0.620	100%	229	0.208	67.18
2	24	1.045	90%	230.7	0.417	79.71
3	24	1.471	80%	233.2	0.625	84.92
4	24	1.898	70%	235.8	0.833	87.73
5	24	2.325	50%	241.6	1.041	89.55
6	24	2.754	40%	244.4	1.248	90.63
7	24	3.185	30%	247.2	1.457	91.49
8	24	3.163	20%	251.4	1.458	92.19
9	24	4.046	10%	308	1.870	92.44

From TABLE IV it is inferred that, when the load resistances is varied, the output voltages are reduced. Because it resists the flow of current and increases the load resistance and Efficiency is also reduced.

TABLE V CLOSED LOOP RESULTS VARIATION IN SUPPLY VOLTAGE

S.NO	V_S(V)	I_S(A)	V_O(V)	I_O(A)	η
1	16	6.701	48	2.076	92.94
2	20	5.371	48	2.081	92.99
3	24	4.478	48	2.079	92.85
4	28	3.852	48	2.079	92.52
5	32	3.399	48	2.082	91.88

TABLE V shows the closed loop analysis of variation in supply voltage. Here the input voltage is changed and constant output voltage is obtained, efficiency is also increased.

TABLE VI VARIATION IN LOAD RESISTANCE

S.NO	V_S(V)	I_S(A)	%LOAD (Ω)	V_O(V)	I_O(A)	η
1	24	0.620	10	48	0.208	67.18
2	24	1.045	20	48	0.417	79.71
3	24	1.471	30	48	0.625	84.92
4	24	1.898	40	48	0.833	87.73
5	24	2.325	50	48	1.041	89.55
6	24	2.754	60	48	1.248	90.63
7	24	3.185	70	48	1.457	91.49
8	24	3.163	80	48	1.458	92.19
9	24	4.046	90	48	1.870	92.44

TABLE VI shows the closed loop variation in load resistances. It is inferred that, when the load resistance is varied, the output voltage is maintained constant. The efficiency increase with increase in load resistancet.

TABLE VII VARIATION IN REFERNCE VOLTAGE

S.NO	V_S(V)	I_S(A)	V_{ref}(V)	V_O(V)	I_O(A)	η
1	24	3.773	44	44	1.905	92.57
2	24	4.478	48	48	2.081	92.94
3	24	5.255	52	52	2.255	92.97

TABLE VII shows the closed loop variation in reference voltages, it is inferred that, when vary the reference voltage, the desired output voltage is obtained. So closed loop control of converter is done for various reference voltages.

VI.CONCLUSION

In this paper, a high gain step-up DC-DC converter is analyzed and designed. From the analysis, it is inferred that, even when there is a variation in supply voltage, load resistance and duty cycle, the desired output voltage is obtained Interleaved SEPIC converter which operates is on both CCM and DCM., we can use This converter For any renewable energy applications can be used to boost up the output voltage and the efficiency of the converter is high.

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