PI Control of Multi Level Inverter Based Shunt Active Power Filter for Harmonic Mitigation in Three Phase Systems

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***Abstract*— Cascaded multilevel inverter is a power electronic device developed to synthesize a desired voltage or current waveforms from several levels of dc voltages making use of its reduced switching stress and modular structure. Such inverters have been recognized as very attractive topologies for implementing shunt active power filters in medium and high voltage applications. This paper presents a five-level cascaded multilevel inverter based Shunt Active Power Filter (SAPF) to compensate reactive power and mitigate the harmonic currents generated by the non-linear loads. The functioning of the proposed system is improved by the inclusion of PI controller for dc-side voltage regulation of SAPF and triangular carrier current controller for the generation of switching pulses for the inverter switches. The control strategy of SAPF also incorporates Synchronous Reference Frame (SRF) theory to extract the harmonic components from distorted line currents which in turn are utilized in the production of required reference compensation currents. This paper primarily focuses on the mitigation of the harmonics produced by the use of non-linear loads with the aid of PI controller for dc voltage regulation. Extensive simulations are carried out to validate performance of the proposed SAPF system using MATLAB/ SIMULINK for diode bridge rectifier with RL load. The dynamic responses of the proposed SAPF system is verified under varying load conditions.**

***Key words* —Cascaded H-Bridge Multilevel Inverter (CHBMLI), Shunt Active Power Filters (SAPFs), Synchronous Reference Frame (SRF) theory, Triangular Carrier Current controller (TCC), Harmonic current compensation.**

I. INTRODUCTION

Increased use of power electronics appliances in industrial, commercial and domestic applications results in rapid variation of reactive power and augmented deterioration of the power systems voltage and current waveforms [1]. The introduction of harmonics in the utility system leads to greater power losses in distribution networks, overloading , overheating and failure of power factor correction capacitors [2]. These systems are more prone to power quality issues as they include microelectronic control systems, which work with very low energy levels [3]. There are several consequences of distortion of the supply network such as

- Harmonic level augmentation resulting from series and parallel resonance.
- Spurious operation of fuses, circuit breakers and protective equipments.
- Reduced product and reduced quality assurance to consumers.

Owing to these problems, the issue of power quality delivered to the end customers is becoming a thing of serious concern. International standards concerning electrical power quality such as IEEE-519, IEC 61000, EN 50160 put forth that electrical equipments and facilities should not produce harmonic currents greater than the specified values and also specify the distortion limits to the supply voltage [4]. Traditionally shunt passive filters, which consists of tuned LC filters are employed to improve power factor and to suppress unwanted harmonics in power systems. Principally, the impedance ratio of the source and the shunt passive filter determines the filtering characteristics of passive filter [5]. As a result, there are certain factors which discourage the use of passive filters such as

- The shunt passive filter which acts as a sink to the harmonic current flowing from the source falls in series resonance with the source impedance .
- Harmonic amplification at specific frequency.
- Component ageing
- Fixed compensation for specific loads.

To overcome the above disadvantages, currently Active Power Filters (APFs) are identified as an appropriate solution for power quality problems.

There are several topologies of active power filters for harmonic mitigation such as series, shunt, series-shunt type (unified power quality conditioner) and hybrid configurations [6]. The series active power filters are employed for voltage harmonic compensation. The necessity of current harmonic compensation in many industrial applications paved the popularity of shunt APFs than series active filters. Among various power circuit topologies for SAPF, Voltage Source

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Inverters (VSI) is an attractive solution to harmonic current problems. Due to the power handling capabilities of power semiconductors, these two-level inverters are limited for low power applications [7]. The harmonic reduction in output waveform without increasing switching frequency or decreasing the inverter power output makes Multi Level Inverters (MLIs) as an ideal suggestion for the power circuit topology of SAPF [8]. With increase in the number of levels, the output voltages of the MLIs have more steps in synthesizing a nearly sinusoidal waveform, thereby reducing harmonic distortion [9]. A multilevel inverter with m-levels , can increase the capacity by (m-1) times than that of two-level inverters through the series connection of power semiconductor devices without additional circuit to have uniform voltage sharing [10]. There are three well known topologies of MLIs [11] : Neutral Point Clamped (NPC) MLI, the Flying Capacitor (FC) MLI and the Cascaded H-Bridge MLI (CHBMLI). The first generation of MLI called NPC multilevel inverter, also called diode-clamped, was introduced by Nabae *et al* [12] which was a three-level inverter. Both NPC and FC MLIs makes use of redundant switching states for the regulation of dc voltage [13].

However, the number of diodes and capacitors increases with increasing the number of voltage levels leading to complicated control scheme. Cascaded MLIs are preferred for harmonic mitigation without having voltage unbalance problem and there are no extra clamping diodes or voltage balancing capacitors [14].In this work, 5-level CHBMLI has been used as the shunt active power filter for harmonic suppression.

To put shunt APF in effective use, it is essential to adopt a suitable control strategy for the extraction of reference compensation currents. Instantaneous active and reactive power theory (p-q theory), unity power factor method, one cycle control, Fast Fourier Techniques (FFT), Fryze power theory are some of the control strategies for reference current extraction in active power filters as given in the literature. H.Akagi put forth p-q theory which is quite efficient method for balanced three phase loads, but this method requires a number of calculations, complex mathematical transformations and suffers from synchronization problems [1]. In 1995, Bhattacharya proposed the calculation of d-q components called Synchronous Reference Frame (SRF) theory which is concise and yields good dynamic performance [15].

The energy loss due to conduction and switching power losses associated with the diodes and MOSFETs of the inverter in APF tend to reduce the value of dc voltage across the dc capacitor. Thus , the maintenance of constant dc voltage across the capacitor connected to the inverter is another important aspect to be considered in the development of active filters. In this work, SRF theory which incorporates PI controller for dc voltage regulation of SAPF is used as an efficient control strategy for reference current extraction of the SAPF. Various PWM current control strategies for shunt active power filter have been proposed in literature [16]. In this work, the switching pulses for the cascaded inverter switches are generated using Triangular- Carrier Current controller (TCC). is paper is organized in five divisions. Commencing with an introduction, the subsequent sections cover configuration of SAPF, the control strategies for SAPF, simulation results of the proposed system and the concluding remarks.

II. Shunt Active Filter Configuration

A. Compensation Principle

The shunt active power filter behaves as a current source injecting the harmonic components generated by the load which are equal but phase shifted by 180^0, which forms the basic principle of SAPF. As a result, components of harmonic currents in the load are cancelled by the effect of shunt active power filter and the source current remains sinusoidal and in phase with the respective voltage. The complete diagrammatic representation of CHBMLI based shunt active power filter is shown in Fig.1. The three phase source is connected to diode rectifier (non-linear) load. The SAPF is realized with 5-level CHBMLI consisting of 24 MOSFETs/Diodes, a dc-side capacitor and RL filter (R_F, L_F) which suppresses the harmonics caused by the switching operation of the MOSFET inverter.

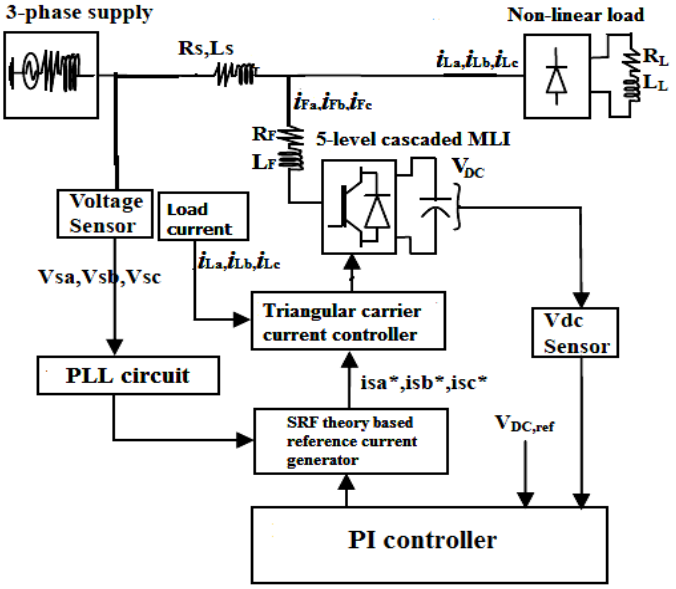

Fig.1 Principle of proposed SAPF system

The control scheme consists of PI for DC voltage regulation, SRF theory for reference current generation and the TCC to spawn the switching pulses for driving switches in the MLI.

B. 5-level Cascaded H-Bridge Multilevel Inverter (CHBMLI)

A 3-phase, 5-level Cascaded H-Bridge Multilevel Inverter (CHBMLI) depicted in Fig.2 is used as the power circuit for shunt active power filter in this work. This inverter requires two, two-leg, series connected H-bridges and four triangular carrier waves [17]. Fig.2 shows two H-bridges connected to a single phase consisting of two parallel legs which has two MOSFETs as a switching device, in a single leg. For a 5-level MLI, m=5, where m is the number of levels in MLI, four carrier waves are required. The output of the current controller

are applied as gating pulses for the inverter switches. The triangular carrier current controller is put in use as it has uniform switching stress for each phase. The MLI has two series connected H-bridges per phase with V_{dci1} and V_{dci2} as two voltages to be regulated, where i corresponds to the three phases (a,b,c) of the inverter. The number of output voltage levels of CHBMLI is given by 2n+1, where n is the number of H-bridges connected in cascade.

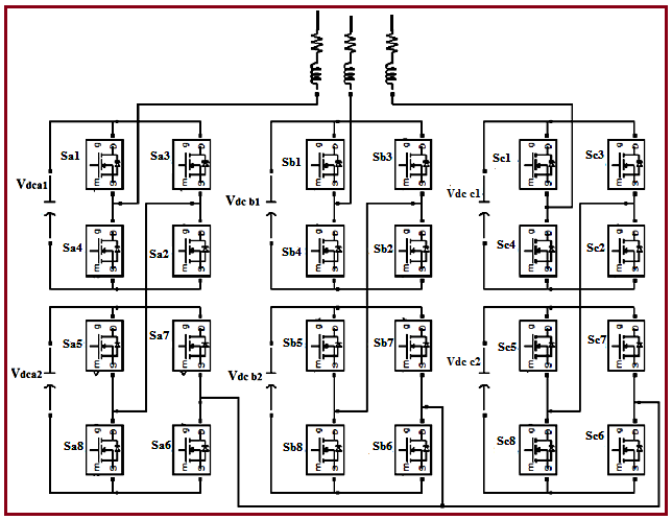

Fig.2. 5-level, Cascaded H-Bridge Multilevel Inverter

III. CONTROL STRATEGIES

A. Reference current extraction

In this work, the time domain based synchronous reference frame theory is utilized to extract the reference current from the distorted line current. Fig.3 shows the basic block diagram of SRF theory consisting of PLL circuit for the generation of unit vectors (sin θ and cos θ) and a controller for dc-side capacitor voltage regulation.

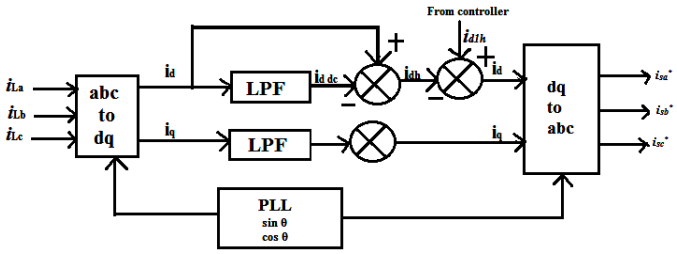

Fig. 3. Block diagram of SRF theory

In this method, the three phase load currents i_{La} , i_{Lb}, i_{Lc} are first detected and transformed into two-phase synchronous (or rotating) frame (d-q axes) using park's transformation as given in Eqn.1.

$$\begin{pmatrix} i_d \\ i_q \end{pmatrix} = \frac{2}{3}\begin{pmatrix} \sin\theta & \sin(\theta-\frac{2\pi}{3}) & \sin(\theta+\frac{2\pi}{3}) \\ \cos\theta & \cos(\theta-\frac{2\pi}{3}) & \cos(\theta-\frac{2\pi}{3}) \end{pmatrix}\begin{pmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{pmatrix} \quad (1)$$

The reference frame is rotating synchronously with fundamental currents. This results in time variant currents with fundamental frequencies which are constant after transformation. Each current component (i_d, i_q) has an average value or dc component and an oscillating value or ac component as shown in Eqn.2.

$$i_d = \overline{i_d} + \tilde{i_d}$$
$$i_q = \overline{i_q} + \tilde{i_q} \quad (2)$$

The i_d and i_q currents obtained from park transformation are passed through a Butterworth type low pass filter to eliminate dc components in the non-linear load currents. To minimize the inverter losses, the required current is added to the positive sequence fundamental frequency active component of the d-q current [18]. Now the currents from two phase synchronous frame are transformed back into three-phase stationary (a-b-c) frame using inverse Park's transformation as per Eqn.3 and the required reference currents are obtained.

$$\begin{bmatrix} i_{Sa}^* \\ i_{Sb}^* \\ i_{Sc}^* \end{bmatrix} = \begin{bmatrix} \sin\theta & \cos\theta \\ \sin(\theta-\frac{2\pi}{3}) & \cos(\theta-\frac{2\pi}{3}) \\ \sin(\theta+\frac{2\pi}{3}) & \cos(\theta+\frac{2\pi}{3}) \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} \quad (3)$$

The obtained reference signals (i_{sa}^*, i_{sb}^* , i_{sc}^*) are compared with the actual load currents in a comparator and the output which acts as the reference signal for triangular carrier current controller. This consequently provides gating signals to trigger the switches of the MLI.

B. DC link voltage regulation

For the APF to work properly, it is essential that the capacitor voltage at the dc-link must remain constant. For this purpose the active power flowing into the active filter needs to be monitored. The dc-link voltage can be maintained at the desired value , if the active power flowing into the filter can be controlled equal to the losses inside the filter. In view of practical implementation, dc-link voltage fluctuations may result from commutation, conductance and own-capacitor losses plus control system delays. The filter operates as a controlled rectifier thereby transferring a little amount of active power from the ac to the dc side of the inverter, for compensating the voltage variations. In order to maintain dc link voltage constant and to generate the compensating reference currents, PI controller is used in this work.

PI controller intended for dc link voltage regulation

The dc-side capacitor voltage is sensed and compared with a set reference voltage. The PI controller which promotes to zero steady state error in tracking the reference current signal, processes the comparison result of the voltage error given by $e = V_{dc\text{-}ref} - V_{dc}$. The output of the PI controller (i_{d1h}) represents the total active current required to maintain V_{dc} at a constant value which in turn compensates for the power losses occurring inside APF represented by Eqn.4 [19].

$$i_{d1h} = K_p.e + K_i \int_0^t e.\,dt \quad (4)$$

where K_p and K_i are the proportional and integral gains of the PI controller respectively. The output i_{d1h} thus obtained is added to the active current in SRF theory to obtain the reference compensating currents.

C. *Triangular carrier current controller*

Most of the current control techniques used for APF are based on PWM-current control strategy. However, the high performance of the current-control is a difficult task in most practical cases, where the inverter load is unidentified and changeable. For the efficient performance of the SAPF, it is essential that the system must supply current in response to the generated reference current. In this work, triangular carrier current controller has been used for the generation of current pulses for the switches of CHBMLI. The reference currents are compared with the actual load currents. This error current is used as the modulating signal and is compared with the four carrier signals in the TCC to produce necessary gating signals for the inverter switches. Fig. 4 shows the current control scheme using TCC for phase 'a' of the CHBMLI.

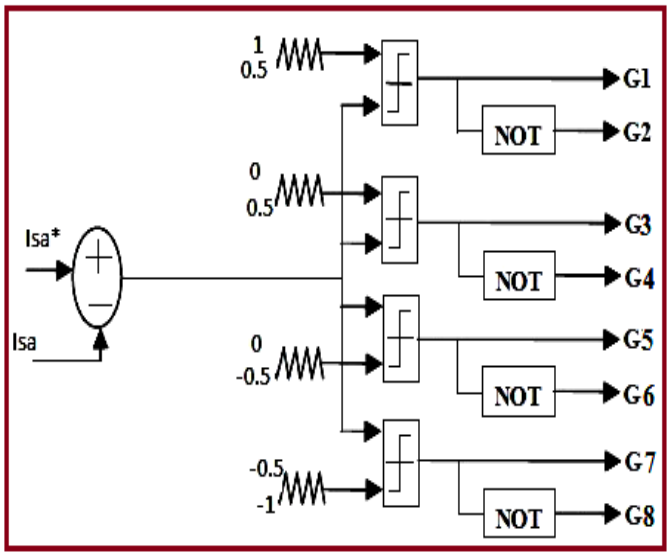

Fig. 4. Current pulse generation for phase 'a' using TCC

IV. Simulation Results

The proposed technique is implemented in MATLAB/SIMULINK working platform to validate the performance of the system using PI controller. The effectiveness of PI controller is proved in terms of THD minimization of source currents before and after compensation. The simulation time is taken as 50 µs and the proposed system is simulated for 0.5s. Here, three phase diode rectifier with RL/RC load is taken as the non-linear load

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A. Simulation results for uncompensated system

Fig.5 shows the source current waveforms before compensation with the SAPF. The corresponding harmonic spectrum is shown in Fig. 6.

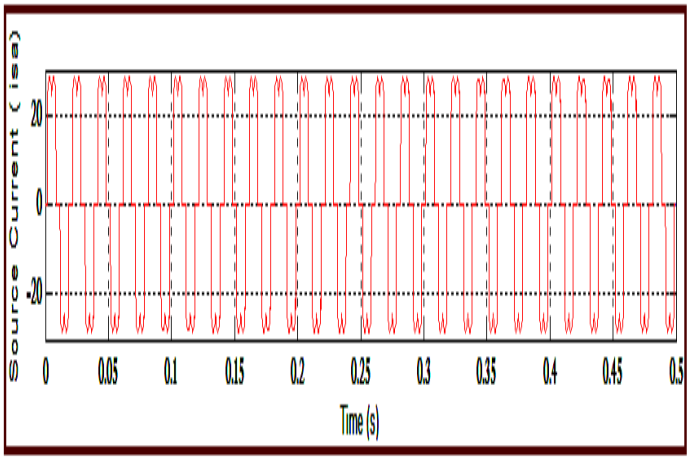


Fig. 5 Source current before Compensation

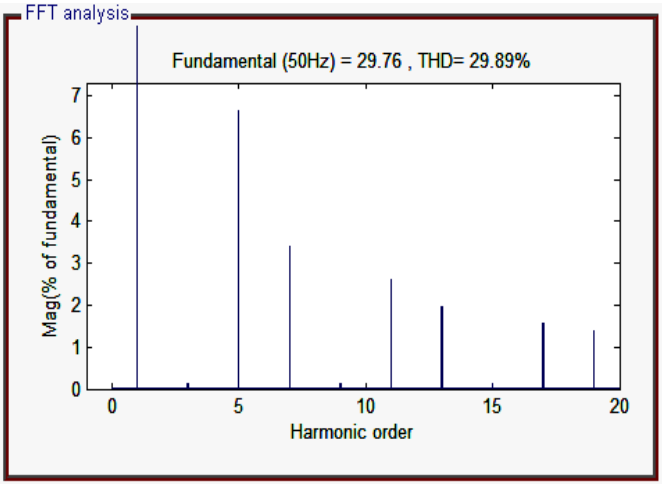


Fig. 6 Source current spectrum for uncompensated system

B. Simulation results with PI controller

The control circuit in SIMULINK model uses SRF theory for reference current generation, TCC for triggering pulse generation and PI controller for dc voltage regulation. The system parameters for simulation are given in Table I. shows The simulation model of SAPF system with PI controller is shown in. Fig.7 The simulated waveforms of source current and injected current after APF application with PI controller are given in Figs. 8 and 9 respectively. The harmonic spectrum of the source current after compensation with PI controller is shown in Fig.10.

TABLE I. SYSTEM PARAMETERS FOR SIMULATION

System Parameters	Values
Phase-phase source rms voltage	440V
System frequency	50 HZ
Source resistor (R_s)	1 Ω
Source inductor (L_s)	0.1mH
Diode rectifier Non-linear load: RL load Load resistor (R_L) Load inductor(L_L) RC load Load resistor (R_L) Load capacitor(C_L)	 20 Ω 10 mH 5 Ω 50 µF
Filter: Inductor (L_F) Resistor (R_F)	 1mH 3 Ω
Dc-side capacitance (C_{DC})	2100 µF
Reference voltage (V_{DCref})	400V
Cascaded multilevel inverter	24- MOSFETS/ diodes

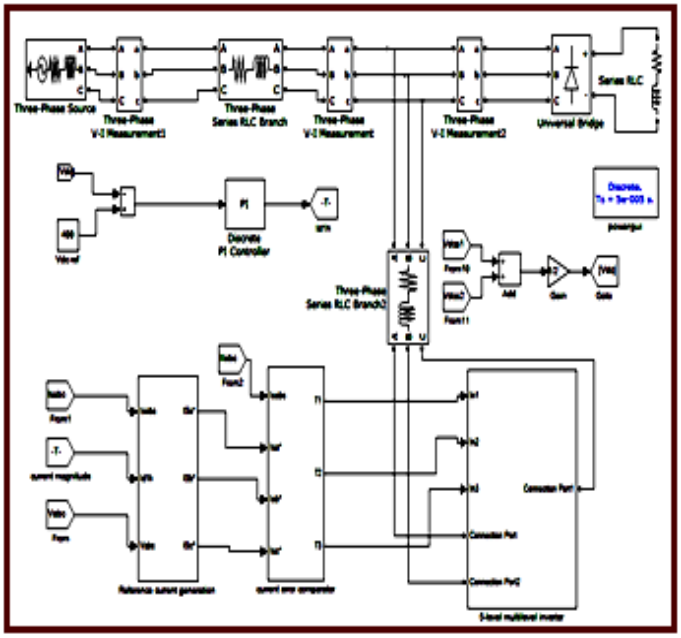


Fig. 7 Simulation model of SAPF system with PI controller

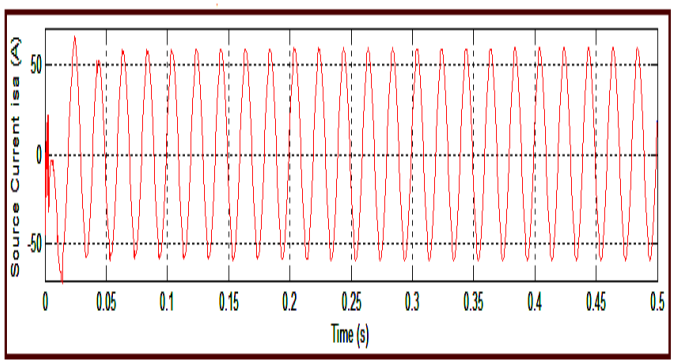


Fig.8 Source current after compensation with PI controller

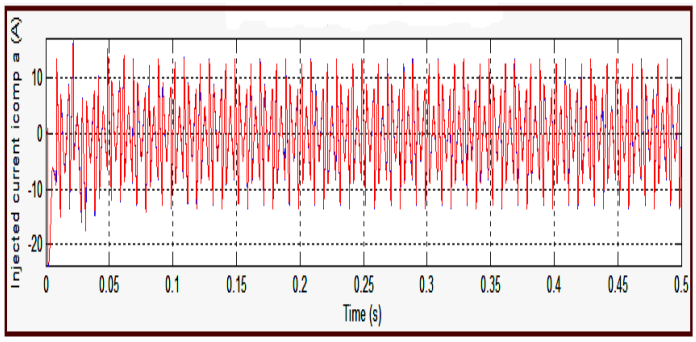


Fig.9 Injected current from SAPF with PI controller

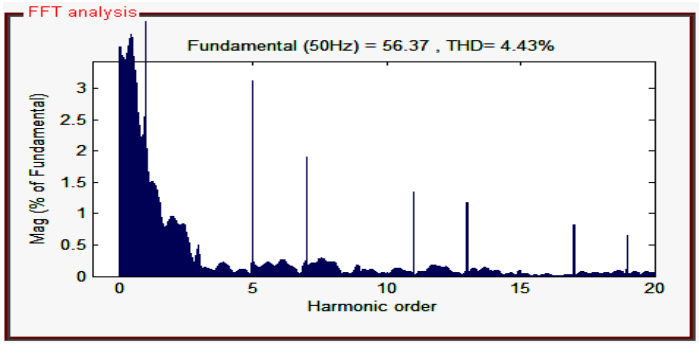


Fig.10 Source current spectrum of SAPF with PI controller THD=4.43%

C. Simulation results using PI controller with sudden step change in load

To evaluate dynamic responses and test robustness of the proposed shunt active power filter a step change is introduced by the use of diode rectifier with RL and RC loads.

Case I. Diode rectifier with RL as non-linear load

The source current using PI controller is shown in Fig. 11. In this initially a RL load of 20 Ω ,10 mH is applied and has a step increase at 0.2s and step decrease at 0.3s. Fig. 12 depicts the simulated harmonic performance for RL load. The source current harmonics is found to be 29.89% without filter and it reduces to 3.89% after compensation with PI controller during initial loading. These results prove the system's dynamic performance during transient condition.

Case II. Diode rectifier with RL as non-linear load

The source current using PI controller is shown in Fig.13. In this initially a RC load of 5 Ω ,50 µF is applied and has a step increase at 0.2s and step decrease at 0.3s. Fig. 14 depicts the simulated harmonic performance for RC load. The source current harmonics is found to be 29.89% without filter and it reduces to 3.88% with PI controller during initial loading. Thus the system's dynamic performance during transient condition is also improved. Table II shows the harmonic performance of simulation with RL/RC loads.

Case III. Unbalanced source voltage condition

` The proposed system is also tested for unbalanced source voltage conditions to test the harmonic performance of the system. In this case, a single phase diode bridge rectifier with RL load is connected to 'a' and 'b' phases to make the source voltage unbalanced. Here unbalance in source voltage is introduced from 0.2s to 0.4s and the corresponding waveforms are shown in Fig.15. From Table III it can be inferred that the harmonics of source currents is found to be 4.6% which comparable to that of performance of the system under unbalanced source voltage conditions.

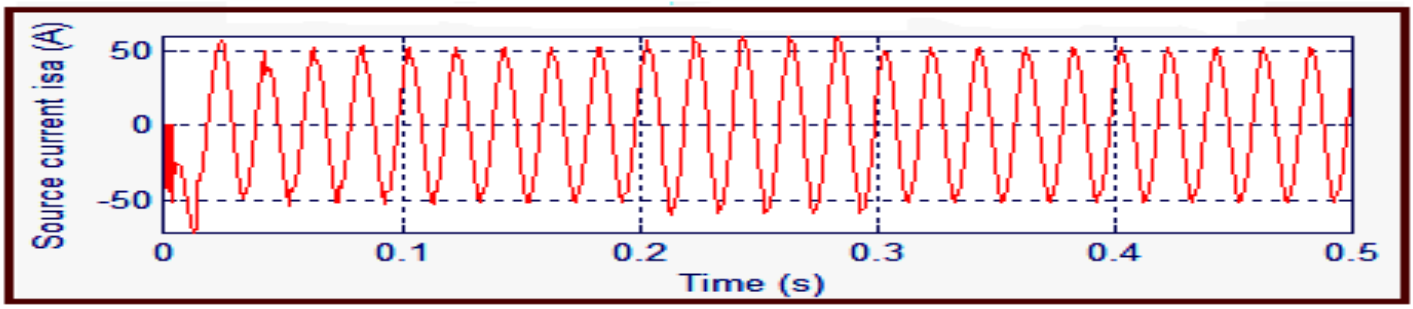
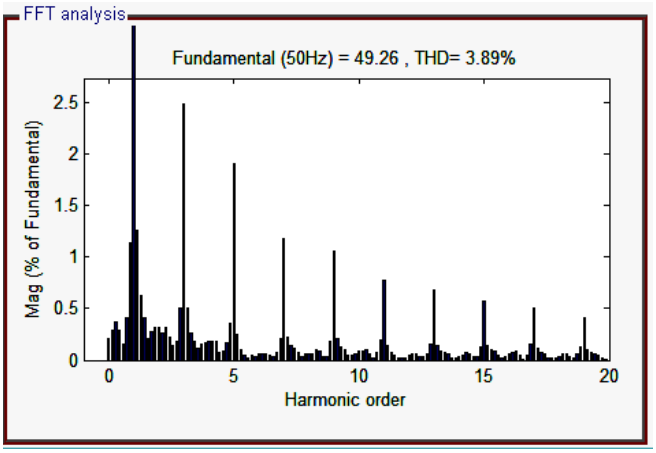
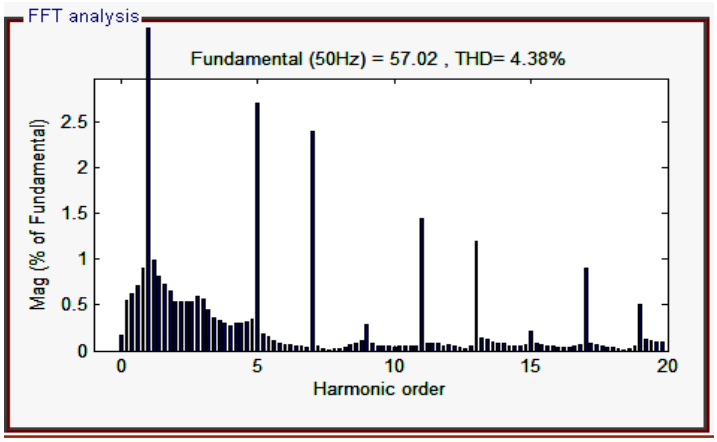


Fig. 11. Source current waveform with step change in RL load (between 0.2s and 0.3s)



(1)



(2)

Fig.12 Simulated harmonics for source current with RL load (1) Initial loading (2) Increase in load

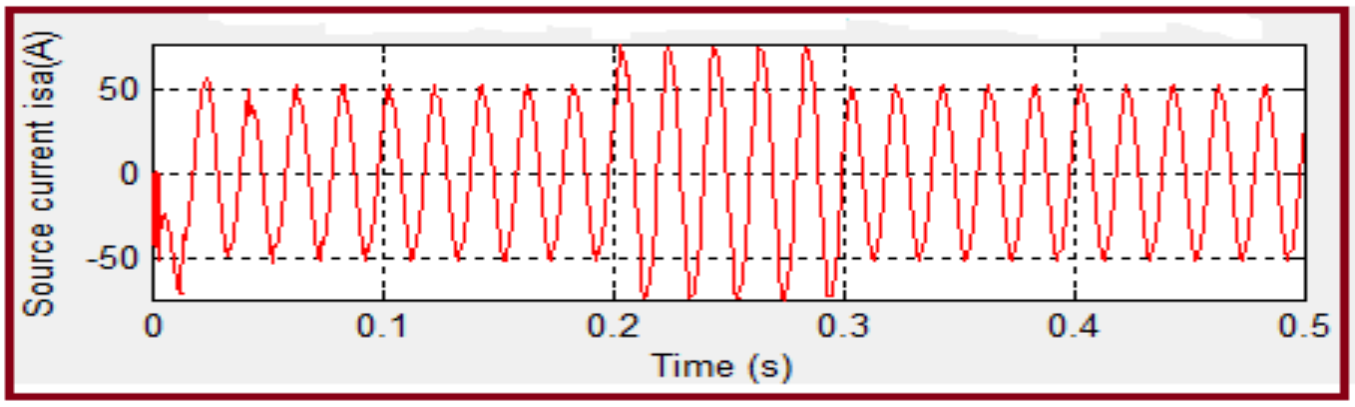


Fig. 13. Source current with step change in RC load (between 0.2s and 0.3s)

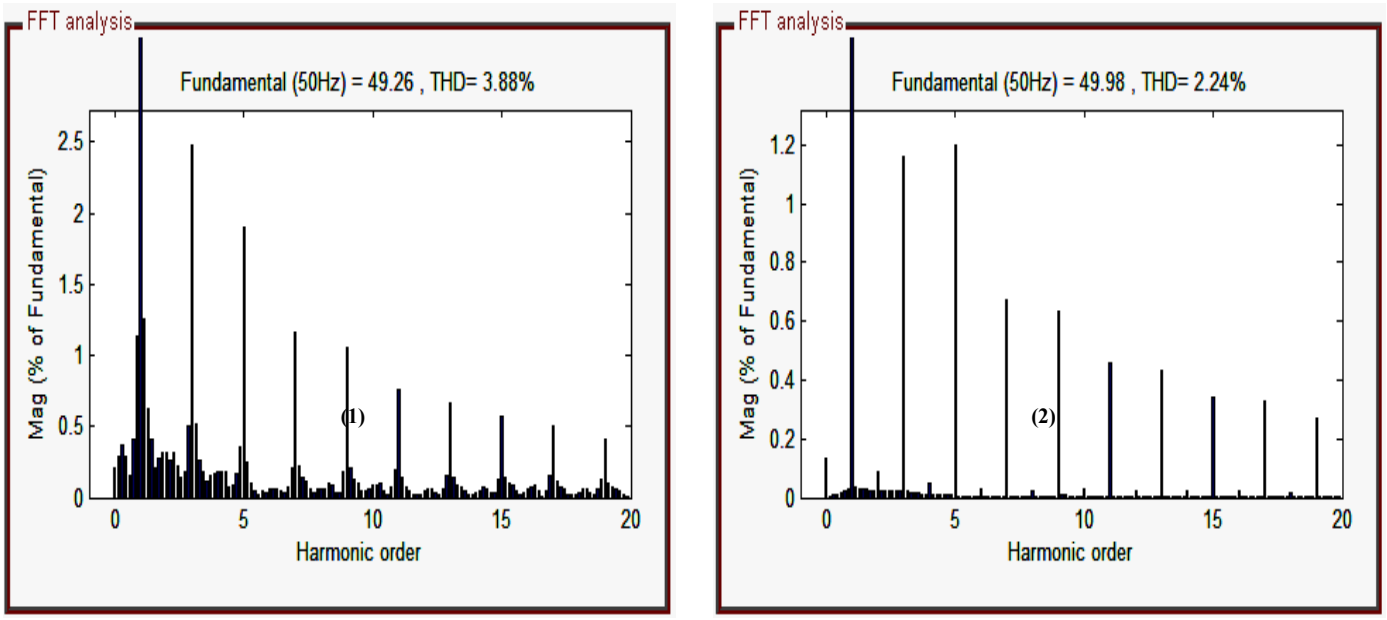


Fig.14 Simulated harmonics for source current with RC load (1) Initial loading (2) Increase in load

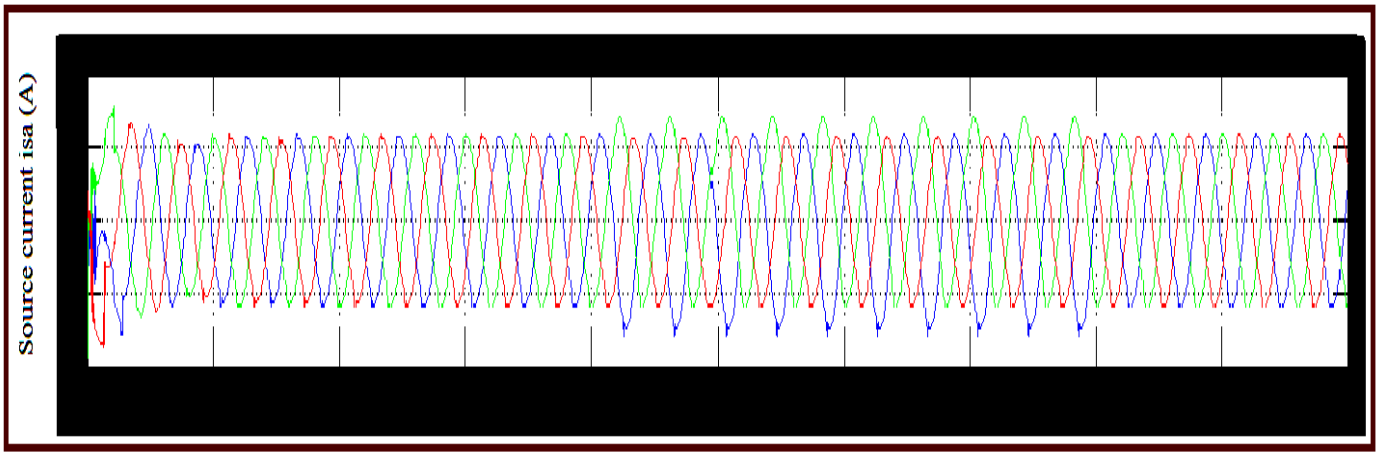


Fig .15 Source current waveforms for unbalanced source voltage

TABLE II HARMONIC PERFORMANCE OF SIMULATION FOR RL/RC LOAD

Time interval (s)	Load condition	Source current THD with PI controller (%)	
		RL Load	RC Load
0.05-0.2	Initial load	3.89	3.88
0.2-0.3	Increase in load	4.38	2.24
0.3-0.5	Decrease in load	3.25	3.24

TABLE III SOURCE CURRENT THD FOR VARIOUS CONDITIONS OF SOURCE VOLTAGE

Phase sequence	Without SAPF	SAPF with PI controller	
		Balanced Source Voltage	Unbalanced Source Voltage
Phase A	29.89%	4.43%	4.6%
Phase B	29.89%	4.43%	4.6%
Phase C	29.89%	4.43%	4.6%

V. CONCLUSION

In this paper, a five-level cascaded H-bridge multilevel inverter based SAPF incorporating PI control for dc voltage regulation is presented. The purpose of this filter is to eliminate the harmonics imposed by non-linear loads. To validate the performance of the proposed system extensive simulations are performed on MATLAB/Simulink platform using diode bridge rectifier with RL/RC load. The simulation results justifies the robustness and effectiveness of the SAPF system with PI controller under varying load conditions and unbalanced source voltage. The THD of source current is significantly reduced from 29.89% to 4.43 % with the utilization of PI controller. The control strategy for reference current extraction based on Synchronous Reference Frame theory provides a better extraction of reference compensation currents from the distorted line current. Thus it is ensured that the proposed SAPF system renders appreciable performance to control shunt active filters based on multilevel inverter topology towards the mitigation of harmonics.

REFERENCES

[1] H. Akagi, Y. Kanazawa, A. Nabae, "Instanataneous Reactive Power Compensator Comprising Switching Devices without Energy Storage Compenents", *IEEE Trans. Industry Applic*., vol. 20, May/June 1984.

[2] Joseph S. Subjak., JR and John S. Mcquilkin "Harmonics - Causes, Effects,Measurements, and Analysis: An Update" *IEEE Trans on Industrial Applications*, vol.26, No.6, pp.1034-1042, Nov/Dec-1990.

[3] Alexander E. Emanuel, John A. Orr, David Cyganski and Edward M.Gulachenski, "A Survey of Harmonic Voltages and Currents at the Customer's Bus" *IEEE Transactions on Power Delivery*, vol. 8, No. 1, pp.411-421, Jan- 1993.

[4] Christopher K. Duffey and Ray. P. Stratford "Update of Harmonic Standard IEEE-519: IEEE Recommended Practices and Requirements for Harmonic Control in Electric Power Systems" *IEEE Trans on Industrial Applications*, vol.25, No.6, pp.1025-1034, Nov/Dec-1989.

[5] Habrouk MEl, Darwish MK, Mehta P., "Active power filters: a review". IEEE Proceedings Electrical Power Applied vol.14, no.5, pp.403–13, 2000.

[6] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, and Zhong Du, "A unified approach to solving the harmonic elimination equations in multilevel converters", *IEEE Transactions on Power Electronics*, vol.19, No.2, pp.278-490, March 2004.

[7] O. Lopez, J. Alvarez, J. Doval-Gandoy, F. D. Freijedo, A. Nogueiras, A. Lago, and C. M. Penalver, "Comparison of the FPGA implementation of two multilevel space vector PWM algorithms," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1537–1547, Apr. 2008.

[8] A.Chen, S. Xie, "Review of the control strategies applied to active power filters", in: Proc. IEEE Int. Conf. on Electric Utility Deregulation, Restructuring and Power Technologies (DRPT-2004), Hong Kong, pp. 666–670, April, 2004.

[9] J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama, "A survey on neutral point clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[10] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, and Zhong Du, "Control of a multilevel converter using resultant theory", *IEEE Transactions on Control Systems Technology*, vol.11, No.3, pp.345-354, May 2003.

[11] B. Suh, G. Sinha, M. D. Manjrekar, and T. A. Lipo, "Multilevel power conversion- an overview of topologies and modulation strategies", *Proceedings of the 6th International Conference on Optimization of Electrical and Electronic Equipments, 1998. OPTIM '98.*, vol.2, pp. AD-11 – AD-24, May 1998

[12] Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

[13] Hirofumi Akagi, Edson hirokazu watanabe and Mauricio Aredes "Instantaneius power theory and applications to power conditioning" IEEE-press chapter 3-4,pp.19-107, 2007.

[14] S. Bhattacharya, D.M. Divan, B. Banerjee, "Synchronous Reference Frame Harmonic Isolator Using Series Active Filter", *Proc. 4th EPE, Florence*, Vol. 3, pp 030-035, 1991

[15] Alabbasi RH, Salih SM. " Control of cascade multilevel inverter using fuzzy logic technique". In: 2nd IEEE International symposium on power electronics for distributed generation systems (PEDG); 2010 pp. 96–101.

[16] Boora, A. Nami, F. Zare, A. Ghosh, and F. Blaabjerg, "Voltage sharing converter to supply single-phase asymmetrical four-level diode clamped inverter with high power factor loads," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2507–2520, Oct. 2010

[17] Alabbasi RH, Salih SM. "Control of cascade multilevel inverter using fuzzy logic technique". In: 2nd IEEE International symposium on power electronics for distributed generation systems (PEDG),pp. 96–101, 2010.

[18] Mikkili Suresh, Panda AK.," PI and fuzzy logic controller based 3-phase 4-wire shunt active filter for mitigation of current harmonics with Id–Iq control strategy". J Power Electron (JPE) (KIPE – South Korea) vol.11,no.6, pp.914–21, 2011.

[19] Y. He, J. Liu, J. Tang, Z. Wang, Yunping Zou, "Research on control system of DC voltage for active power filters with three-level NPC inverter," IEEE, pp.1173-1178, 2008.